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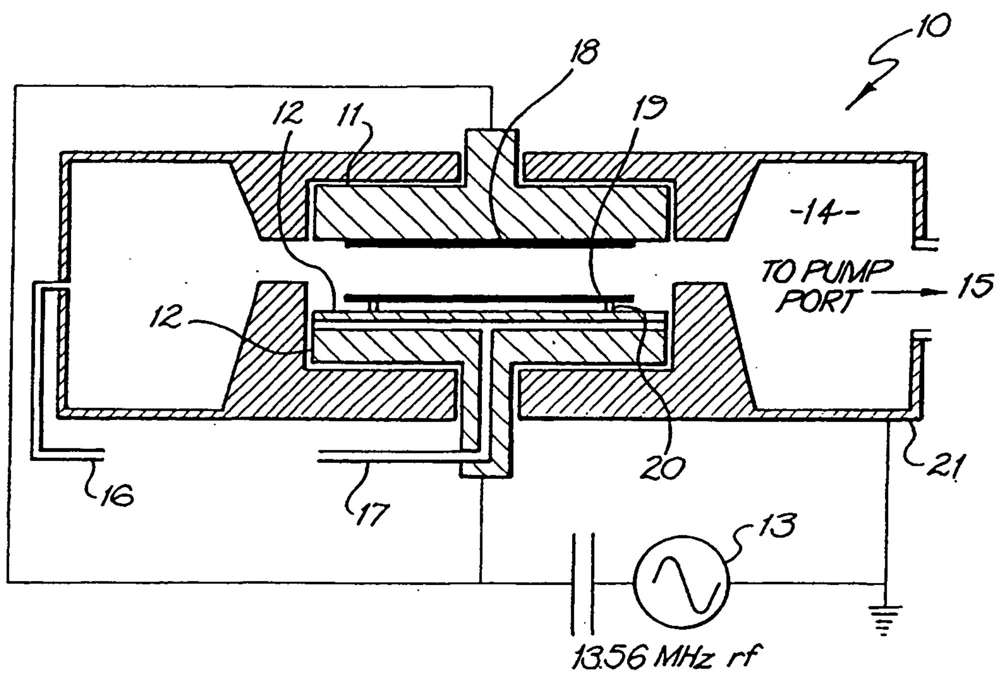

(57) Abstract

The invention relates to a method for etching of silica–based layers/substrates by reactive ion etching system (10) using an etching gas mixture of CHF_3/AR through a photoresist mask. Reactive ion etching is carried out under conditions of simultaneous isotropic deposition of a carbon–based polymer where the polymer deposition rate is controlled by adjusting process control parameters of RF power, sample temperature, O_2 and CF_4 additions.

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Reactive Ion Etching of Silica Structures

Field of the Invention

The present invention relates to creation of silica structures and in particular to the reactive ion etching of such structures.

Background of the Invention

Silica-based channel waveguides, fabricated on silicon or silica wafer substrates, are potential building blocks of planar lightwave circuits (PLCs) that are becoming increasingly important for telecommunications systems. While there are a number of thin film techniques that have been used to deposit silica waveguiding layers (flame hydrolysis, chemical vapour deposition and plasma enhanced chemical vapour deposition (PECVD)), almost all reported waveguide fabrication schemes have used reactive ion etching (RIE) to delineate the channel waveguide (core) geometry. RIE is also commonly used in integrated optics, and in planar waveguide fabrication in particular, for etching light turning mirrors. It further finds use in the creation of other Micro Electro Mechanical Systems (MEMS).

RIE of silica glass in integrated circuit (IC) manufacture is a well established and routine process with, for example, CHF_3 based mixtures being used to obtain high selectivity over photoresist. Although basically similar, the silica films used in planar waveguides have several unique differences which influence the development of suitable RIE processes. Firstly, the thicknesses of silica in waveguide devices can be as much as 5 to 10 μm, as opposed to typically less than 1 μm in IC technology. This places extra demands on mask thickness and/or material selectivities, as well as on the silica etch rate which should be high enough to obtain reasonable throughput. Different masking materials for waveguide etching such as photoresist, amorphous silicon (a-Si) and chromium have been reported. Generally, the use of non-photoresist masks allows for larger etching depths and silica etch rates.

The roughness of the etched walls of the waveguide structures or light turning mirrors should ideally be as small as possible in order to reduce the loss due to light scattering. A number of works on sidewall roughness reduction for etching with photoresist masks have been reported. In these cases, however, the etching depth of a SiO_2 layer was restricted to around 1 µm. Etched profile control is also important and some slope in the etched profile is sometimes desirable in order to facilitate filling of the gaps between closely spaced waveguides during cladding deposition. Profile slope is normally achieved by controlled photoresist mask erosion. Despite a number of published works on different aspects of the RIE of silica for waveguide fabrication, it is unclear as to the effect of all relevant parameters, such as etch rates, sidewall roughness, profile slope and the relationship between them.

Summary of the Invention

It is an object of the present invention to provide for the development of a high-rate silica RIE process suitable for low temperature waveguide fabrication.

In accordance with the first aspect of the present invention there is provided a method for etching of silica-based glass layers or substrates comprising reactive ion etching through a mask executed under conditions of simultaneous isotropic deposition of a carbon based polymer.

Preferably, the polymer deposition rate or/and its steady-state thickness on different surfaces of the etched structure is controlled by adjusting one or several process control parameters in order to control etched profile, dimension loss, sidewall and bottom etched surface roughness, and etching selectivity between the silica-based layer and mask material.

A gas or a mixture of gases containing fluorine or carbon atoms is used and a photoresist mask or other form of mask such as amorphous silicon. Adjustable parameters can include RF power and substrate temperature. The temperature

can be adjusted to achieve low sidewall roughness and low dimension loss at the same time. Further, resputtering of any metal present wihtin or/and in contact with the discharge zone can be prevented.

The invention is ideally suited wherein reactive ion etching is performed in a high plasma density hollow cathode etching system and the etching gas mixture is CH_3F and Argon.

Various products made utilizing the previous methods are also disclosed.

In accordance with a further aspect of the present invention there is provided a high plasma density hollow cathode etching system is disclosed which has been shown to provide higher etch rates than those achievable in previously known standard RIE systems. Etching was carried out in a CHF_3/Ar mixture with additions of O_2 and CF_4. The effects of the different chemistries as well as the use of different masks (photoresist and amorphous silicon) and the effects the substrate temperature on etching rates, sidewall roughness and etch profiles have been investigated. Using a photoresist mask generally results in greater sidewall roughness compared to an amorphous silicon mask. Importantly, polymer deposition during the etching process can exacerbate the development of roughness but is still desirable to a certain extent in the prevention of the loss of line width during etching. Two mechanisms of polymer deposition control are disclosed, namely, the addition of varying amounts of O_2 or CF_4, and elevating the temperature of the substrate. The latter was found to give a good compromise between control over the line width loss and the sidewall roughness. In order to explain the variety of experimental results obtained, a simple phenomenological model based on a polymer etching/deposition rate equilibrium on etched surfaces is proposed and examined.

<u>Brief Description of the Drawings</u>

Notwithstanding any other forms which may fall within

the scope of the present invention, preferred forms of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 is a schematic illustration of the basic layout of hollow cathode discharge chamber used in the preferred embodiment.

Fig. 2a to Fig. 2g illustrate graphs of etch rates and selectivities over mask material for etching with a-Si (Fig. 2a) and photoresist (Fig. 2g) masks as a function of RF power. Pressure is 12 Pa. Gas flow rates: 60 sccm of Ar, 15 sccm of CHF_3. Sample temperature is 80°C.

Fig. 3a to Fig. 3d illustrate graphs of etching profile slope (Fig. 3a) dimension loss (Fig. 3b), sidewall roughness (Fig. 3c) and polymer deposition rate (Fig. 3d) as a function of RF power for etching with a-Si and photoresist masks. The pressure is 12 Pa. The gas flow rates: 60 sccm of Ar, 15 sccm of CHF_3. The sample temperature is 80°C. The dimension loss was normalized to an etching depth of 5 μm. The polymer deposition rate was measured in the area shielded from ion bombardment.

Fig. 4a to Fig. 4h are Electron microscope images of etching profiles as a function of RF power for etching with a-Si (Fig. 4a to Fig. 4d) and photoresist masks (Fig. 4e to Fig. 4h). The RF power was as follows: Fig. 4a- unetched a-Si mask, Fig. 4b- 250W, Fig. 4c-500W, Fig. 4d-650W, Fig. 4e-unetched photoresist mask, Fig. 4f-300W, Fig. 4g-400W, Fig. 4h 500W. Pressure is 12 Pa. Gas flow rates: 60 sccm of Ar, 15 sccm of CHF_3. Sample temperature 80°C.

Fig. 5a to Fig. 5e illustrate graphs of etch rates and selectivities with Fig. 5a to 5c illustrating SiO_2 etch rates and selectivities over an a-Si mask and Fig. 5d to Fig. 5e illustrating vertical and lateral etch rates of a-Si mask as a function of sample temperature, for a O_2 flow rate and a CF_4 flow rate, respectively. RF power is 500W. Pressure is 12 Pa. Gas flow rates: 60 sccm of Ar, 15 sccm of CHF_3. Sample temperature 80°C unless varied.

Fig. 6a to Fig. 6j illustrate graphs of the etching profile slope (Fig. 6a to Fig. 6c) sidewall roughness (Fig. 6d to Fig. 6f) and polymer deposition rate (Fig. 6g to Fig. 6j) as a function of sample temperature, O_2 flow rate and CF_4 flow rate, respectively using an a-Si mask. RF power is 500W. Pressure is 12 Pa. Gas flow rates: 60 sccm of Ar, 15 sccm of CHF_3. Sample temperature 80°C unless varied. Polymer deposition rate was measured in the area shielded from ion bombardment.

Fig. 7a and Fig. 7b illustrate electron microscope images for etched sidewalls for sample temperature 80° (Fig. 7a) and 320°C (Fig. 7b). The a-Si mask is still in place. RF power is 500W. Pressure is 12 Pa. Gas flow rates: 60 sccm of Ar, 15 sccm of CHF_3.

Fig. 8 illustrates a sectional view of a wafer showing the four possible etched surfaces with respect to intensity of ion bombardment and the possibility of polymer film formation: the surfaces include (i) the top surface of the mask 31, (ii) the sidewalls of the mask 32, (iii) the sidewalls of SiO_2 33 and, (iv) the bottom surface of the SiO_2 34. A steady state thickness of polymer film can be present on (i-iii), whereas (iv) is assumed polymer free under the etching conditions used in this study.

Fig. 9a to Fig. 9c are electron microscope images of time evolution of the etched profile: with Fig. 9a showing an unetched a-Si mask, Fig. 9b after 3 minutes etching, Fig. 9c after 6 minutes etching. RF power is 500W. Pressure is 12 Pa. Gas flow rates: 60 sccm of Ar, 15 sccm of CHF_3. Sample temperature is 80°C. Etching selectivity over the a-Si mask is approximately 14:1. A "negative undercut" is shown to be developed without mask width reduction. The more vertical profile of the a-Si mask is "buried" under polymer formed at a steady state angle determined by the polymer etching and deposition equilibrium.

Fig. 10 is a schematic illustration of a mechanism of sloped profile formation. A steady state profile angle 0°

is formed under conditions where $Er_{polymer} = Dr_{polymer}$. For this angle the steady state thickness of polymer film on the sidewall is enough to prevent etching. The no-zero polymer etch rate at 0 = 90° is due to ions scattered in plasma sheath.

Fig. 11a and 11b illustrate etched sidewalls for etching with a photoresist mask (Fig. 11a) and a a-Si mask (Fig. 11g). Pressure is 12 Pa. Gas flow rates: 60 sccm of Ar, 15 sccm of CHF_3. Sample temperature is 80°C. RF power is 500W for etching with the photoresist mask and 650W for etching with the a-Si mask.

Description of Preferred Embodiments

A first embodiment of the present invention relies upon the utilisation of plasma enhanced chemical vapour deposition (PECVD) in a hollow cathode discharge chamber. Turning initially to Fig. 1 there is shown a suitable vacuum chamber assembly 10 including a top electrode 11 and a bottom electrode 12 connected as shown to RF source 13 which comprised a 13.56 MHz RF source. In use for the purposes of PECVD, the chamber 14 is evacuated via pump port 15 and gases such as CH_4/SF_6 mixtures, CHF_3/Ar mixtures are introduced via corresponding ports e.g. 16, 17, so as to cause controlled etching on wafers or substrates 19 located in the RF field induced plasma located between electrodes 11, 12. This apparatus 10 is utilised to perform the controlled ion etching operation as discussed in detail below.

The high plasma-density hollow cathode discharge etching system suitable for use is described in C.M. Horwitz, S. Boronkay, M. Gross and K.E. Davies, J. Vac. Sci. Technology A6, at pages 1837 to 1844 (1988). The two opposing RF powered parallel circular electrodes 11, 12 are surrounded by a grounded chamber 21. A conventional diode discharge is produced between each of the electrodes 11, 12 and the grounded chamber 21 but a high density plasma is generated between the two RF powered electrodes 11, 12 due

to the "electron mirror" effect. Both the upper and lower electrodes were water-cooled and covered with 100 mm diameter silicon wafers 18, 19. The latter is to prevent resputtering of the electrode material (Al) which can result in metal contamination and subsequent surface roughness and the formation of sloped etching profiles due to metal-based polymer deposition. Examination of the polymer deposited in the ion-shielded areas (as described below) using wavelength dispersive X-ray spectroscopy (WDS) showed that no traces of Al or other vacuum chamber materials could be detected at the 0.01 % level, thus confirming that metal contamination is not an issue.

The silica films used in the etching experiments had a thickness of 8 µm and were deposited on silicon substrates 19 using the hollow-cathode PECVD technique. Masking layers of 1 µm of PECVD a-Si or 2 µm of photoresist were then applied to the wafer 19. The photoresist mask was patterned using conventional photolithography, while patterning of the a-Si layer was carried out using conventional photolithography followed by etching in a CF_4/SF_6 mixture.

In each run the samples 19 were etched to a depth of around 4-5 µm, with the rates determined by surface profilometry. The etched profile, sidewall roughness and dimension loss were further determined by SEM examination. The dimension loss was calculated or defined as the difference between the line width measured at the bottom of the mask before etching and the width at the top of the etched ridge. When determining the sidewall roughness, the SEM photos were taken from the top side of the ridge, at a glancing angle to the sidewall. Sidewall roughness figures set out hereinafter are the average amplitudes of the RIE-induced corrugations measured over a distance of a few microns. The initial (unetched) roughness of both the photoresist and a-Si mask edge was not larger than 0.02 µm.

The silica films were etched in a 20 % CHF_3 in Ar mixture with various additions of CF_4 or O_2. The pressure was

kept at 12 Pa in all experiments. All gases had a stated purity of 99.95 % or better. Etching in CHF_3 was accompanied by some polymer deposition. The polymer deposition was estimated using a shadowing technique, whereby the polymer deposition is assumed to be isotropic. An overhanging structure consisting of two overlapping silicon wafers was used and the thickness of polymer deposited under the overhang (and so shielded from ion bombardment) was measured using surface profilometry.

The temperature of the samples was controlled by varying the thermal contact between the sample 19 and the cooled electrodes eg. 12. For an A-Si mask, three cases were characterized by thermocouple measurements: (i) no thermal contact between the sample and the electrode; (ii) partial thermal contact through several point contacts of vacuum grease; (iii) good thermal contact through vacuum grease spread on the back of the sample. Good thermal contact was used in all experiments where the temperature was held constant and for all photoresist masked samples.

Results

The Effect of RF Power

Etch rates: The resulting etch rates as a function of RF power (at 13.56 MHz) coupled into the discharge are shown in Fig. 2a for an a-Si mask and in Fig. 2b for a photoresist mask. It is seen that the SiO_2 etch rate is slightly higher (around 10 %) in the case of the a-Si mask for similar power levels. With the a-Si mask the SiO_2 etch rate increases by almost a factor of three over the investigated power range reaching a value of 0.8 μm/min at the maximum power. The a-Si etch rate increases with power faster than the SiO_2 etch rate thus causing an overall decrease in selectivity over a-Si from 20:1 to 12:1. Similarly, the selectivity over photoresist also decreases with the power.

Etched profile and dimension loss: The etched sidewall slope angle, as a function of power for a-Si and photoresist masks, is shown in Fig. 3a. The SEM photographs of the

corresponding etched profiles are shown in Figs. 4a to 4h. For both mask materials the angle of the profile slope was found to increase with the power, being greater for an a-Si mask for similar power levels. The dimension loss (Fig. 3b) (normalised to a depth of 5 μm) for the a-Si mask was found not to exceed 0.2 μm (although it seemed to increase slightly with power), at the same time the dimension loss for the photoresist mask was quite significant (>1 μm) and clearly increased with power as illustrated in Fig. 3b. This difference probably points to different mechanisms being responsible for the sloped profile formation in both cases. It may be noted from Figs. 4a to 4h, where the initial mask profiles before etching are shown, that a facet is developing on the photoresist mask sidewall, thus possibly contributing to the observed dimension loss.

Sidewall roughness: As illustrated in Fig. 3c, the sidewall roughness appears to be consistently higher for a photoresist mask than for an a-Si mask. In both cases, however, it was found to increase with power and, as can be seen in Fig. 3c, the sidewall roughness for etching with an a-Si mask at the highest power level is comparable with the sidewall roughness obtained with the photoresist mask at lower power levels.

Polymer deposition rate: The polymer deposition rate in the area shadowed from ion bombardment was found to give results as indicated in Fig. 3d. It was found to increase by about 30 % over the whole power range. Also, it may be noted that at the minimum power, the polymer deposition rate was around 3 times smaller than the SiO_2 etch rate, which means that in ion bombarded areas, during etching of 1 μm of SiO_2, around 0.35 μm of polymer is simultaneously removed. As the power increases this portion of removed polymer is reduced to around 20 % or 0.2 μm for 1 μm of SiO_2.

The Effect of O_2 and CF_4 Additions, and Sample Temperature Variation

As polymer deposition was found to play an important

role in the etching mechanism, different methods of controlling it were investigated. These include (i) O_2 additions, (ii) CF_4 additions and, (iii) elevated substrate temperature.

Etch rates: Figs. 5a to 5f show SiO_2 and a-Si etch rates and selectivity plotted on the same scales for all three varied parameters. It is seen that the SiO_2 etch rate decreases with temperature and O_2 additions, but increases with CF_4 additions. At the same time the selectivity over a-Si decreases in all three cases. The a-Si mask etch rate shown in Figs. 5a to 5f has been separated into two components, a vertical component, which is related to the mask thickness decrease, and a lateral component, which is related to the mask width decrease. It can be seen from that under the conditions of no O_2 or CF_4 and a low sample temperature (80°C), the lateral etch rate is essentially zero (<80Å/min). At elevated temperature and with O_2 added it stays initially at around zero but then rises, ultimately approaching the vertical etch rate values, which implies isotropic etching of the a-Si mask. For CF_4 the behaviour is different, the lateral etch rate increases gradually but the mask etching remains basically anisotropic. With increases in all three parameters the vertical a-Si etch rate increases which, together with a decrease in the SiO_2 etch rate at higher temperatures and O_2 additions, and a slower rate of increase with CF_4 additions, results in an overall decrease in selectivity.

Etched profile: As illustrated in Fig. 6a, the slope of the etching profile was found to first increase with temperature and then decrease below the initial value. As shown in Fig. 6b, O_2 additions caused a small initial increase in the slope followed by a gradual decrease. As illustrated in Fig. 6c, the slope was found to be essentially independent of the CF_4 flow rate.

Sidewall roughness. As shown in the sidewall roughness was found to decrease with both temperature (Fig. 6d) and O_2

flow (Fig. 6e) but was not effected by the CF_4 (Fig. 6f). It is seen that the sidewall roughness can be reduced to 0.02 µm, either by elevating the sample temperature or by adding O_2 to the gas mixture. However, by comparing Fig. 6d with Fig. 5a and Fig. 5d, it can be seen that, using temperature as a control parameter, minimum sidewall roughness can be achieved while maintaining the anisotropy of the a-Si mask etching. O_2 can also be used to reduce roughness (Fig. 6e), but the same minimum roughness can only be achieved at the expense of dimension loss, since, at the required O_2 flow rates, the etching of a-Si becomes essentially isotropic (Fig. 5e). From a practical point of view this suggests that the sample temperature is a more useful control parameter for reducing sidewall roughness compared to the addition of O_2. The improvement in the sidewall roughness can be seen in Figs. 7a and 7b, which shows SEM images of two sidewalls etched at different temperatures.

Polymer deposition rate: The polymer deposition rate on a shadowed surface as a function of sample temperature, O_2 flow rate and CF_4 flow rate, is shown in Fig. 6g, Fig. 6h and Fig. 6j, respectively. It is seen (Fig. 6g) that by increasing the temperature, the polymer deposition is first reduced and then, with a further increase in the temperature, is totally suppressed, which means that there is no polymer deposition above a certain sample temperature even in absence of ion bombardment. O_2 additions (Fig. 6h) cause only a small decrease in the polymer deposition rate, which is noteworthy given the similar effect of temperature and O_2 on the sidewall roughness. This may indicate a difference in the mechanisms by which the two parameters reduce the sidewall roughness. Finally it is seen from Fig. 6j that the polymer deposition rate increases with C_4 flow by about 25 % of its initial value.

It is evident from the aforegoing analysis that essentially isotropic polymer deposition occurs

simultaneously with etching. Furthermore, the formation of polymer films under similar etching conditions, with thicknesses depending on an equilibrium between the polymer etch and deposition rates, has been demonstrated in a number of other investigations.

Turning to Fig. 8, in the case of the etched structures described it is possible to specify four surfaces 31 - 34 on which such a film may exist. Previous investigations using similar conditions have shown that SiO_2 surfaces 34 are free of polymer film for RF bias voltages above 100V (at a pressure of 0.13 Pa), and that the threshold bias voltage between polymer etching and deposition decreases with pressure. Therefore, using 12 Pa and 400V - 600V bias, a polymer free SiO_2 bottom surface 34 generally results. This is supported by the fact that SiO_2 etch rates do not increase with polymer suppression, either by O_2 additions, or increasing sample.

Temperature (Fig. 5a and 5b). Thus, a polymer film can be present only on surfaces 31, 32 and 33. The polymer on surface 31 determines the etching selectivity, whereas 32 and 33 will effect the etching profile and sidewall roughness. The presence of a finite thickness of polymer implies that both etching species and reaction products must diffuse through the polymer on their way to or from the etched surface, a mechanism which has previously been suggested by others. Here, in addition to etching of the polymer film by normal surface process, it is assumed that etching species diffusing through the polymer film have a certain probability of reaction with the polymer, which is proportional to the film thickness. Porosity in the polymer film can contribute to this etching mechanism. As the polymer film thickness increases, this "diffusion" etching component also increases, thus increasing the total polymer removal rate and preventing continuos film growth. For a constant polymer deposition rate, these effects will give rise to a certain equilibrium polymer thickness, which will

determine the etch rates of the underlying surfaces.

While not wishing to be bound by theory, a simplified phenomenological model describing this mechanism can be written as follows:

$$ER \propto I_a (1-\alpha d) \leq 1 \quad \text{(EQ.1)}$$

$$ER_{polymer} \propto c_1 I_a \alpha d + c_2 I_i Cos(\phi)\, Y(I_a, E_I, \phi), \alpha d \leq 1 \quad \text{EQ.2}$$

$$DR_{polymer} \propto \gamma\ (T) I_p \quad \text{(EQ.3)}$$

where ER is the etch rate of the surface under the polymer film, I_a is the flux of active etching species at the polymer film surface, α is the probability of polymer etching by diffusing active species per unit of film thickness, d is the thickness of the polymer film, $ER_{polymer}$ is the polymer etch rate, C_1 and C_2 are empirical constants, I_i is the ion flux, ϕ is the sidewall slope or effective ion angle of incidence, $Y(I_a, E_i, \phi)$ is the reactive sputtering yield as a function of active species flux I_a, ion energy E_i and effective ion angle of incidence ϕ. I_p is the flux of polymer forming species and $\gamma^{(T)}$ is the sticking probability of the polymer forming species as a function of the surface temperature. The photoresist, a-Si and SiO_2 etch rate results of Figs. 2 and 3 can be explained using this model.

The observed decrease in etching selectivity over both photoresist and a-Si with power of Fig. 2a and Fig. 2b can be explained by a decrease in the steady-state polymer thickness on both mask surfaces 31, 32 (the SiO_2 surface is assumed polymer free). This occurs in spite of the increasing polymer deposition rate with power (Fig. 3d). According to Eq. (2) above this means that the increase in polymer deposition rate is overshadowed by the increase in both reactive sputter etching and "diffusion" etching components, thus requiring a smaller polymer thickness to

maintain the polymer etching/deposition equilibrium.

Increasing temperature, O_2 flow and CF_4 flow all reduce the etching selectivity over a-Si, mainly through a greater vertical a-Si etch rate (Fig. 3). Again, since the SiO_2 surface 34 is assumed to be polymer free, this implies a decrease in the polymer thickness on a-Si. Increasing temperature reduces the sticking probability of the polymer forming species with causes a reduction in the polymer deposition rate according to Eq. 3. This is also confirmed by Fig. 6g where the polymer deposition rate in the area shielded from ion bombardment is shown to decrease with temperature. The polymer thickness then decreases (Eq. 2) causing and increase in a-Si etch rate through Eq. 1. In the case of O_2 additions is not significant (Fig. 6h). Similarly, CF_4 additions lead to a reduction in the polymer thickness despite a small increase in the polymer deposition rate (Fig. 6j). In this case, however, the a-Si etch rate can increase, not only because of a reduction in polymer thickness, but also due to an increase in the active species flux, resulting from CF_4 dissociation.

While the vertical a-Si etch rate increases in response to all three factors (temperature, O_2 and CF_4), the lateral a-Si etch rate behaves differently for the temperature and O_2 cases on one side and CF_4 case on the other (Fig. 5d to Fig. 5f). For increasing temperature and O_2 flow the lateral etch rate increases, approaching the vertical etch rate, thus indicating isotropic etching of the a-Si mask. In the case of CF_4 additions, however, the lateral a-Si etch rate increase is small and the anisotropy remains unchanged due to a proportional increase the vertical etch rate.

According to Eq. 1, the difference in vertical and lateral etch rate of the a-Si mask is due to the different steady-state polymer film thickness on its top surface and sidewalls. The sidewalls receive less ion bombardment during etching which, according to Eq. 2, reduces the reactive sputtering component of polymer etching and causes

an increase in its steady-state thickness to the point where lateral etching of the mask ceases, as seen in the first few points in Fig. 5d to Fig. 5f. The increasing lateral etch rate with temperature and O_2 additions is due to a reduction in polymer thickness on the sidewalls. In the temperature case, this can be attributed to reduced polymer deposition Fig. 6g. In the O_2 case, where the polymer deposition rate data show only a small decrease Fig. 6g, the similar reduction in sidewall polymer thickness is due to higher polymer removal rate by active oxygen. The absence of polymer on the sidewalls for high O_2 flow rates, as opposed to its presence in the areas shielded from ion bombardment Fig. 6j is likely to be due to some ion bombardment on the mask sidewalls by ions scattered in the sheath (characteristic for the operating pressure around 10 Pa employed which is, although relatively small, apparently enough to initiate polymer etching by the products of O_2 dissociation).

The addition of CF_4, although causing an increase in the vertical a-Si etch rate in a way similar to increased temperature and O_2, does not alter the ratio of the vertical to lateral etch rates. According to the model this implies that some polymer film remains on both the sidewalls and top surface of the a-Si mask, with its steady state thickness on both surfaces reduced proportionally with the CF_4 additions.

Finally, we note that, despite there being no polymer on the a-Si mask surface at high temperature or high O_2 flows, its vertical etch rate, although increased, still remains around 5 times smaller than the SiO_2 rate. This suggests that the well accepted mechanism of SiO_2 etching, where the SiO_2/Si selectively is due to selective polymer removal by oxygen released from the SiO_2 during etching, is accompanied by an additional mechanism in this case. That is, under conditions of intense ion bombardment, the production of CHF_3 dissociation apparently etch SiO_2 faster than Si, even when there is no protective polymer film on

the Si surface.

Sidewall angle

A sloped profile in silica, a material with known intrinsically anisotropic etching characteristics may be produced in two ways. The first mechanism, mask erosion, produces a sloped profile through lateral mask etching. This is well documented in the literature and may be deliberately induced by, for example, addition of O_2 when using a photoresist mask. The considerable dimension loss observed when using a photoresist mask (Fig. 3b) suggests that mask erosion is the cause of the sloped profile in this case. The reason for high lateral photoresist mask etching, in the light of similar selectively to SiO_2 as a-Si, is probably the result of faceting of the photoresist mask edge. This can be seen in Fig. 4a to Fig. 4h where the photoresist mask is shown before and after etching. From the round shape before etching (Fig. 4e) the mask sidewall becomes flat and sloped (Fig. 4h) at the preferential sputtering angle. An estimate of the lateral etching rate of the photoresist mask due to faceting is around 1000 Å/min, which is more than twice the vertical etch rate. The increase in slope angle with power observed for a photoresist mask can be attributed to the preferential increase in the SiO_2 sidewall etch rate compared to the increase in the lateral mask etch rate. Here, the SiO_2 sidewall is not protected by polymer, since the angle is less than the steady-state value required for polymer film formation.

The effect of the second mechanism of sloped profile formation can be seen in Fig. 9a to Fig. 9c where the time evolution of an etched silica profile is shown starting with an unetched a-Si mask (Fig. 9a). Here, it can be seen that the width of the mask has not changed, but the effective linewidth has increased, rather than decreased as is the case of mask erosion. This effect, which has been termed "negative mask undercut" or "overcut" can occur under

conditions of anisotropic etching of the substrate and mask in the presence of a simultaneous isotropic deposition process.

The SiO_2 sidewall etch rate is zero when all the etching species are consumed in the sidewall polymer film before reaching the SiO_2 surface, or when $\alpha d = 1$ (Eq. 1). The steady-state polymer thickness required to satisfy this condition is found when $ER_{polymer} = Dr_{polymer}$. However, since both the ion flux to the sidewall and the angular dependence of the reactive sputtering yield depend on the sidewall slope, the etching rate of the sidewall polymer will depend on the slope (ϕ in Eq. 2). Thus, assuming isotropic polymer deposition, there is a sidewall angle ϕ_o, at which $ER_{polymer}(\phi_o) = DR_{polymer}$, and hence zero SiO_2 sidewall etch rate. If the angle were greater than this equilibrium value then the reactive component of polymer etching would be lower, $DR_{polymer} > ER_{polymer}$, and net deposition would occur. Conversely, if the angle were less than the equilibrium value, then the reactive component of polymer etching would be higher, $DR_{polymer} < ER_{polymer}$ and net etching would occur. This mechanism is shown graphically Fig. 10. The point 41 where the semicircle 40 representing isotropic polymer deposition crosses the line 42 representing the angular dependence of the polymer etch rate corresponds to the angle at which the polymer etching/deposition balance is achieved. This angle is the steady-state angle of the SiO_2 sidewall 44. The angular dependence of the polymer etch rate in Fig. 10 is drawn schematically and includes both the angular dependence of the ion flux on the sidewall $I_i Cos(\phi)$ and the angular dependence of the sputtering yield, $Y(I_a, E_i, \phi)$ the latter having a maximum around 60°. As the polymer deposition rate (the semicircle radius 45) increases, the intersection between it and the angular dependence curve 42 (the polymer etching/deposition equilibrium point) shifts upwards thus decreasing the sidewall angle. Similarly, if the polymer

etch rate increases, the intersection shifts downwards and the angle increases. This mechanism can be applied to explain the experimental data.

The etched profile observed using an a-Si mask is seen to be "overcut" (Fig. 3b and Fig. 9a to Fig. 9c). The effect of higher power is to increase the reactive sputtering component of polymer etching due to higher ion energy and density.

According to the above mechanism, this establishes a new polymer etching/deposition equilibrium at a higher sidewall angle, as observed. The increase in polymer deposition rate, which also occurs with power (Fig. 3d) is apparently less than the increase in its etch rate.

One can explain the profile slope dependences on temperature, O_2 and CF_4 additions in similar terms, keeping in mind the a-Si mask lateral etch rate tendencies (Fig. 5a to Fig. 5f). The profile slope initially increases with temperature and with O_2 flow (although only slightly) and then decreases in both cases Fig. (6a and Fig. 6b). The initial increase in the slope profile versus temperature is due to a decrease in polymer deposition through a reduced sticking probability of polymer forming species. The new deposition/etching equilibrium occurring at a higher angle according to Fig. 10. In the case of O_2 flow, the polymer deposition rate decreases only slightly but its reactive sputtering rate increases due to active oxygen produced in the discharge thus increasing the equilibrium sidewall angle. Further increases in temperature and O_2 flow cause total polymer removal from the sidewalls of the a-Si mask, resulting in lateral etching of the a-Si and a smaller sidewall angle due to mask erosion. The sidewall slope is relatively independent of CF_4 additions, which indicates that the increase in polymer deposition rate due to CF_4 flow is balanced by the simultaneous increase in its etching rate, probably due to an increase in the fluorine flux.

<u>Sidewall Roughness</u>

Since the initial mask-edge roughness, determined by SEM examination of both a-Si and photoresist masks, was significantly smaller than the post-etch sidewall roughness, this can be eliminated as a source of the observed sidewall roughness. Thus, either the mask edge is roughened during etching, or the roughness is formed on the silica sidewall itself. Both these occurrences can result from micromasking in the presence of ion bombardment and polymer deposition. Since the photoresist masked samples were cooled, photoresist reticulation is not an issue.

Fig. 11a shows a etched sidewall with a photoresist mask still in place. It is seen that roughness has been generated in the photoresist during the process and then transferred to the silica sidewall where the mask edge has been thinned by the faceting which is evident. The increase in silica sidewall roughness with power can be explained by an increase in micromasking as both ion bombardment and polymer deposition rate increase.

In the case of an a-Si mask (Fig. 11b), some of the observed sidewall roughness may be produced by mask roughening, as can be deduced from Fig. 11b, which shows an etched sidewall with the a-Si mask still in place. However, while there is some faceting of the top corner of the mask, the upper part of the sidewall close to the mask is smoother than the lower part, suggesting that a larger part of the roughness has not been transferred from the mask edge, but rather has formed on the sidewall during etching. The reason for this additional roughness is likely to be the sidewall polymer which can act as a micromasking material. The sidewall roughness increase with power can be explained by an increase in micromasking, in this case in both the mask edge and the sidewall itself, as both ion bombardment and polymer deposition rate increase.

Both increased sample temperature and O_2 additions reduce roughness (Fig. 5d and Fig. 5e). In both cases this is likely to be the result of sidewall polymer suppression.

In the temperature case, as a result of a reduction of the polymer deposition rate to zero (Fig. 6g), and in the O_2 case through an increase in the polymer etch rate. In the absence of sidewall polymer, this contribution to micromasking induced roughness is eliminated. The sidewall roughness does not change with CF_4 additions (Fig. 6f), which is consistent with the fact that the profile slope also does not change, since the latter implies an unperturbed balance between polymer etching and deposition and therefore a constant polymer thickness on the sidewalls.

Trade off between sidewall roughness and dimension loss

Using the sample temperature as a control parameter allows smooth sidewalls to be obtained without dimensional loss, whereas using O_2 additions does not allow for a process window where both dimension control and smooth sidewalls can be achieved. In the O_2 case, active oxygen enhances the polymer etching rate on both the a-Si mask and SiO_3 sidewalls and therefore, together with an improvement is sidewall roughness, it brings about dimension loss due to isotropic etching of the mask. In the case of increasing sample temperature, the flux of polymer forming species from the plasma remains unchanged, but their sticking probability is reduced, thus decreasing the effective polymer deposition rate, which then results in reduced roughness. However the results obtained here suggest that with increasing temperature the sticking probability of polymer forming species to silica is reduced faster than to the a-Si surface. This can allow for polymer free SiO_2 sidewalls and simultaneously, sufficient polymer remaining on the a-Si mask sidewalls to prevent dimension loss.

It can be seen from the forgoing, the application of reactive ion etching of silica in a high plasma density hollow cathode etching system to the fabrication of silica based integrated optic devices can be effectively utilised. This application imposes specific requirements on the etching depth, sidewall roughness and profile slope control.

Due to the high plasma density produced in the hollow cathode discharge, high silica etch rates (over 0.5µm for a-Si) and significant dimension losses (>1µm for 5µm etching depth). The disadvantages with photoresist are believed to originate from strong faceting which occurs on the mask sidewall. In a-Si mask the faceting is negligible. Increasing RF power results in a decrease in selectivity and an increase in sidewall roughness for both photoresist and a-Si masks.

The effects of sample temperature an the addition of CF_4 and O_2 on the etching characteristics for an a-Si case have been investigated. The etching selectivity is reduced with all three parameters. Increasing sample temperature and O_2 content permit sidewall roughness reduction to 0.02µm. However, in the O_2 case, the reduction in sidewall roughness is accompanies by lateral etching of the a-Si mask causing dimension loss and a decrease in the profile slope. A similar effect observed with the sample temperature, however in this case there appears to be a temperature range where smooth sidewalls can be obtained, together with almost vertical sidewalls and without dimension loss.

Finally based on polymer deposition rate measurements, a model explaining the variety of experimental data is explained. The model is based on a balance between isotropic polymer deposition and etching. A polymer film of a certain steady-state thickness is formed as a result of this balance on (i) the top surface of the mask, (ii) the sidewalls of the mask and (iii) the sidewalls of the SiO_2. The polymer thickness on the top surface determines the etching selectivity, whereas the polymer thickness on the mask sidewalls and SiO_2 sidewalls determines the profile slope and sidewall roughness.

In conclusion, the silica reactive ion etching process of the preferred embodiment satisfies all the requirements of planar waveguide fabrication and can also be used for other integrated optics applications or MEMS applications

where deep etching of silica is required along with smooth etched sidewalls and vertical or sloped etching profiles.

It would be appreciated by a person skilled in the art that numerous variations and/or modifications may be made to the present invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

We Claim:

1. A method for etching of silica-based glass layers or substrates comprising reactive ion etching through a mask executed under conditions of simultaneous isotropic deposition of a carbon based polymer.

2. The method of claim 1 wherein the polymer deposition rate or/and its steady-state thickness on different surfaces of the etched structure is controlled by adjusting one or several process control parameters in order to control etched profile, dimension loss, sidewall and bottom etched surface roughness, and etching selectivity between the silica-based layer and mask material.

3. The method of any previous claim wherein gas or a mixture of gases is used, which contain fluorine and carbon atoms.

4. The method of any previous claim wherein a photoresist mask is used.

5. The method of claims 1 to 3 wherein a non-photoresist mask is used.

6. The method of claim 5 wherein amorphous silicon is the mask material.

7. The method of any previous claim wherein the RF power coupled into the discharge is the adjusted parameter.

8. The method of any previous claim wherein the substrate temperature is the adjusted parameter.

9. The method of claim 8 where the temperature is adjusted to achieve low sidewall roughness and low dimension loss at the same time.

10. The method of any previous claim wherein a resputtering of any metal present wihtin or/and in contact with the discharge zone is prevented.

11. The method of any previous claim wherein reactive ion etching is performed in a high plasma density hollow cathode etching system.

12. The method of any previous claim wherein the etching gas mixture is CH_3F and Argon.

13. A product made by the method of any previous claim.

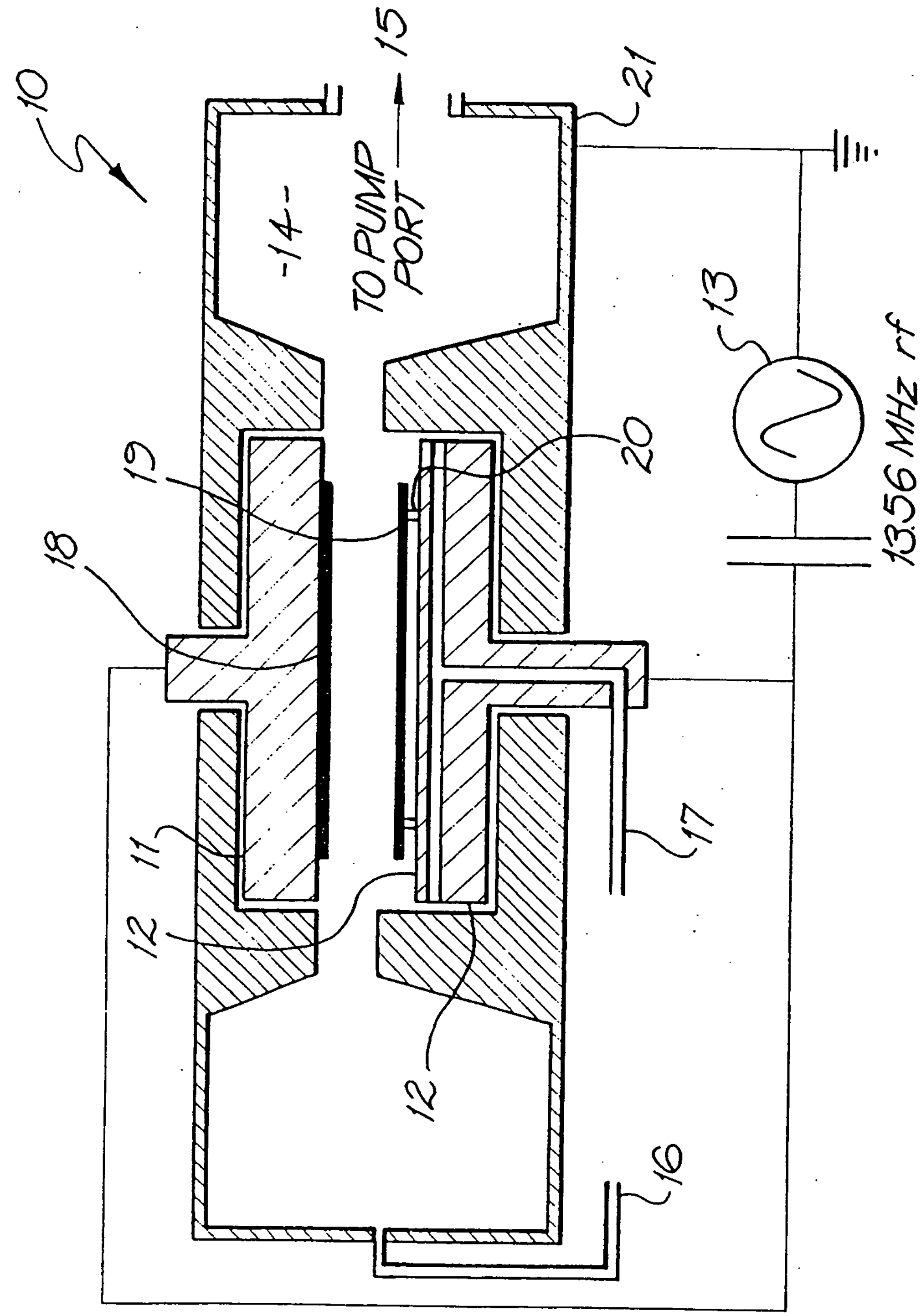


FIG. 1

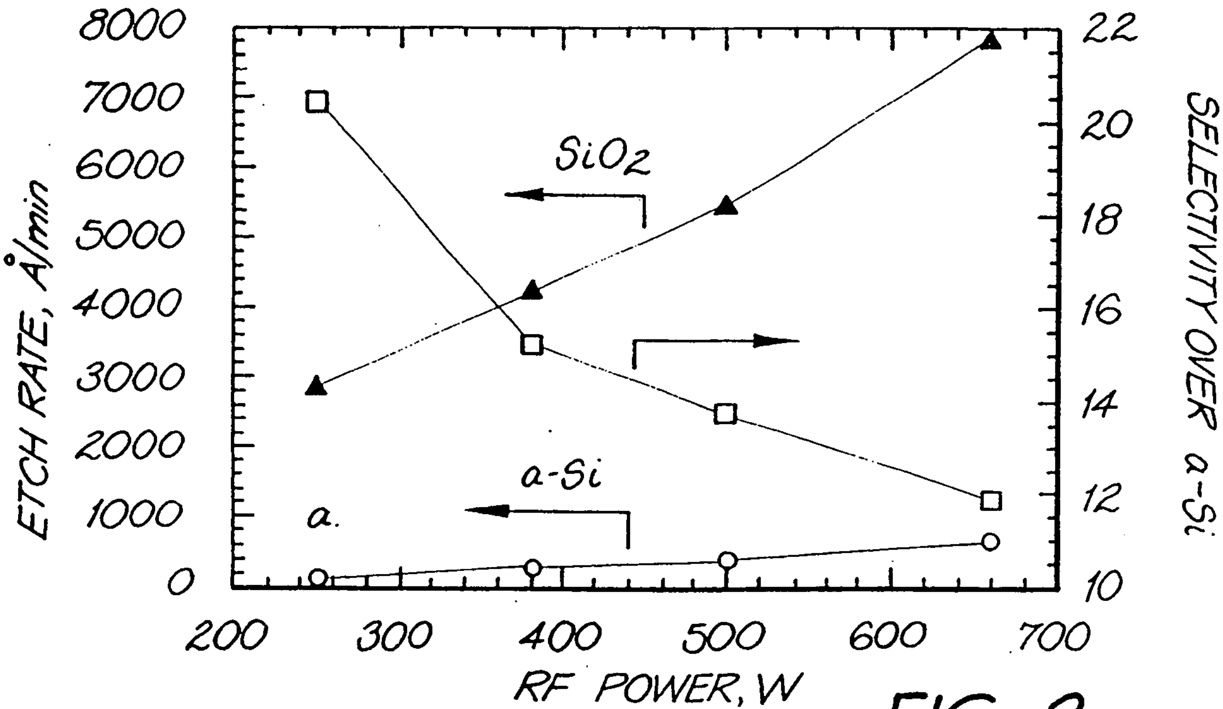

8000
7000
6000
5000
4000
3000
2000
1000
0
ETCH RATE, Å/min
SiO_2
a-Si
a.
22
20
18
16
14
12
10
SELECTIVITY OVER a-Si
200
300
400
500
600
700
RF POWER, W

FIG. 2a

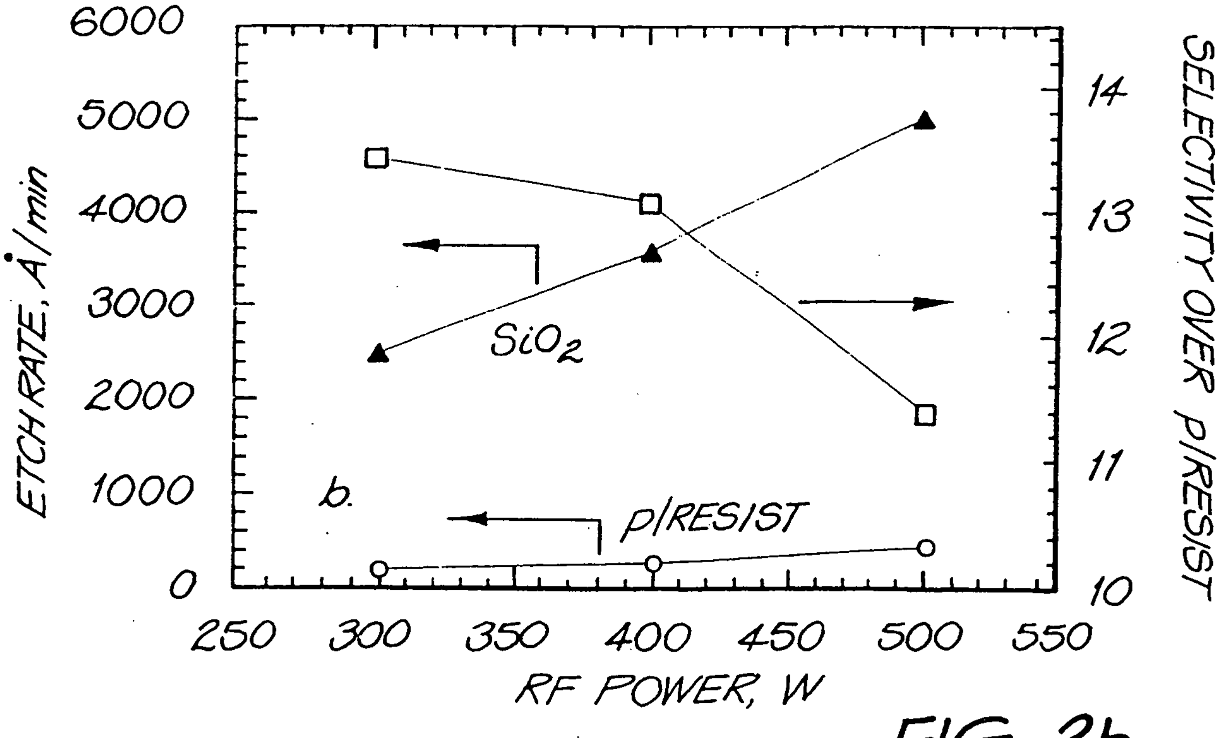

6000
5000
4000
3000
2000
1000
0
ETCH RATE, Å/min
SiO_2
b.
p/RESIST
14
13
12
11
10
SELECTIVITY OVER p/RESIST
250
300
350
400
450
500
550
RF POWER, W

FIG. 2b

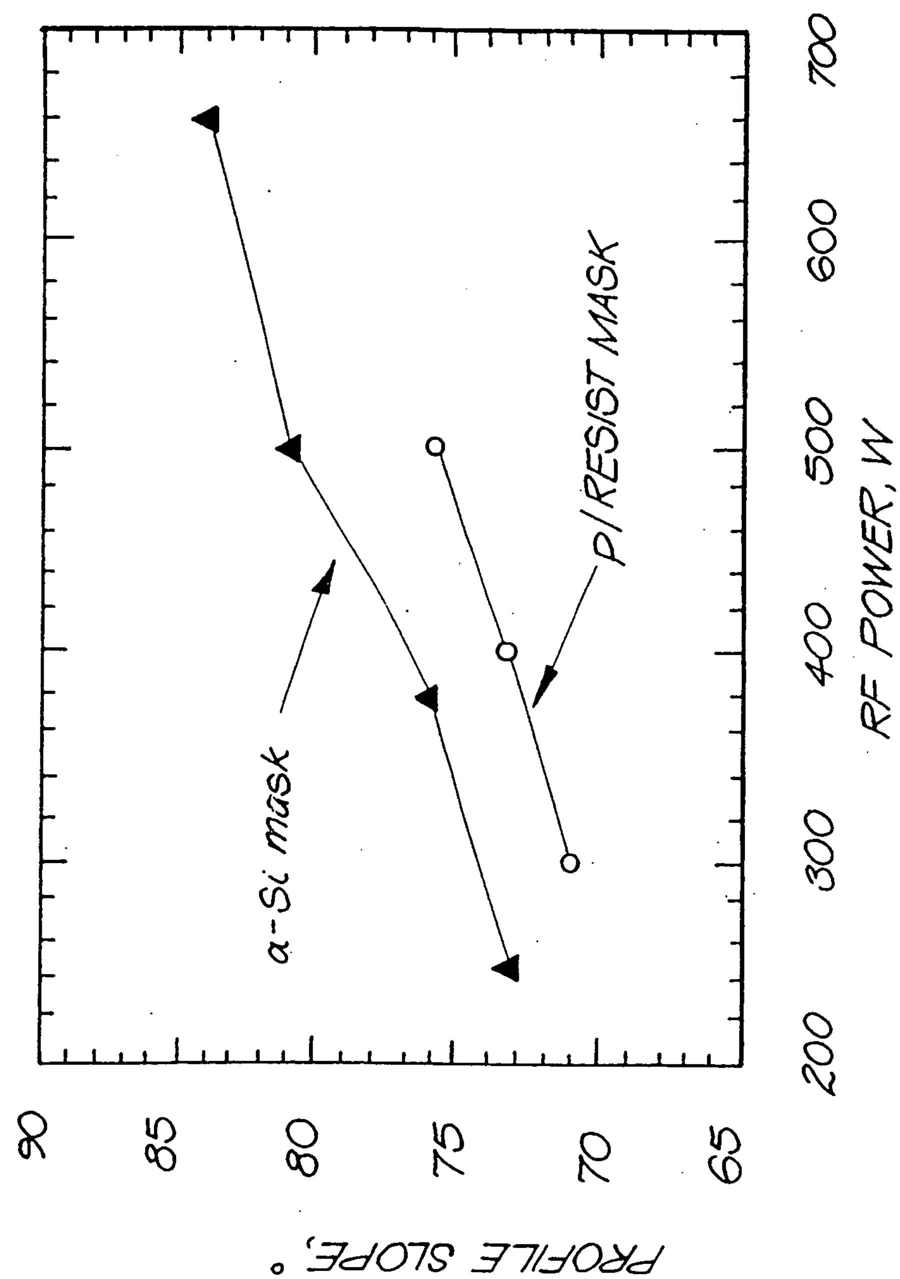

PROFILE SLOPE, °
90
85
80
75
70
65
200
300
400
500
600
700
RF POWER, W
a-Si mask
P/RESIST MASK

FIG. 3a

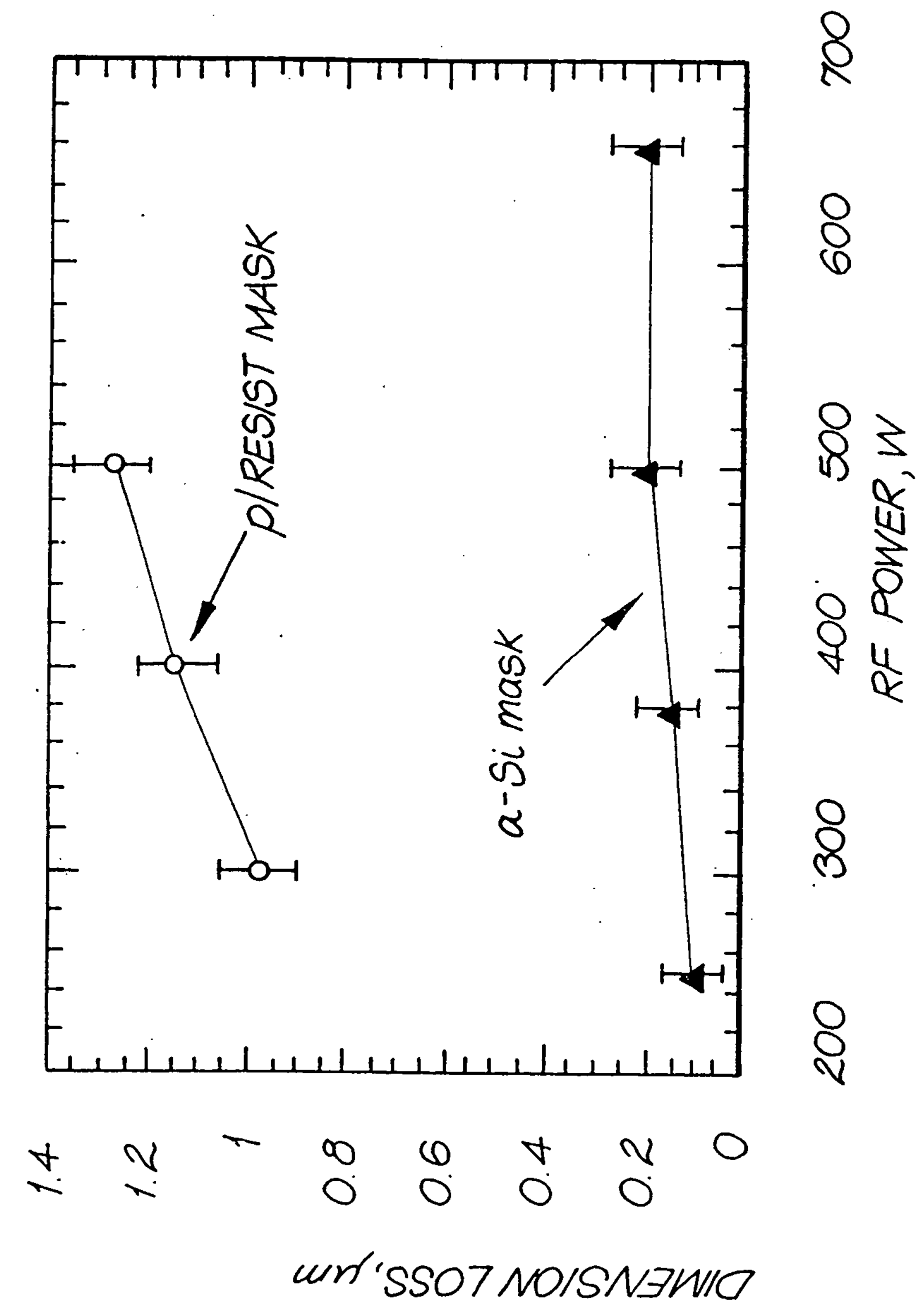

p/RESIST MASK
a-Si mask
RF POWER, W
200
300
400
500
600
700
DIMENSION LOSS, µm
0
0.2
0.4
0.6
0.8
1
1.2
1.4

FIG. 3b

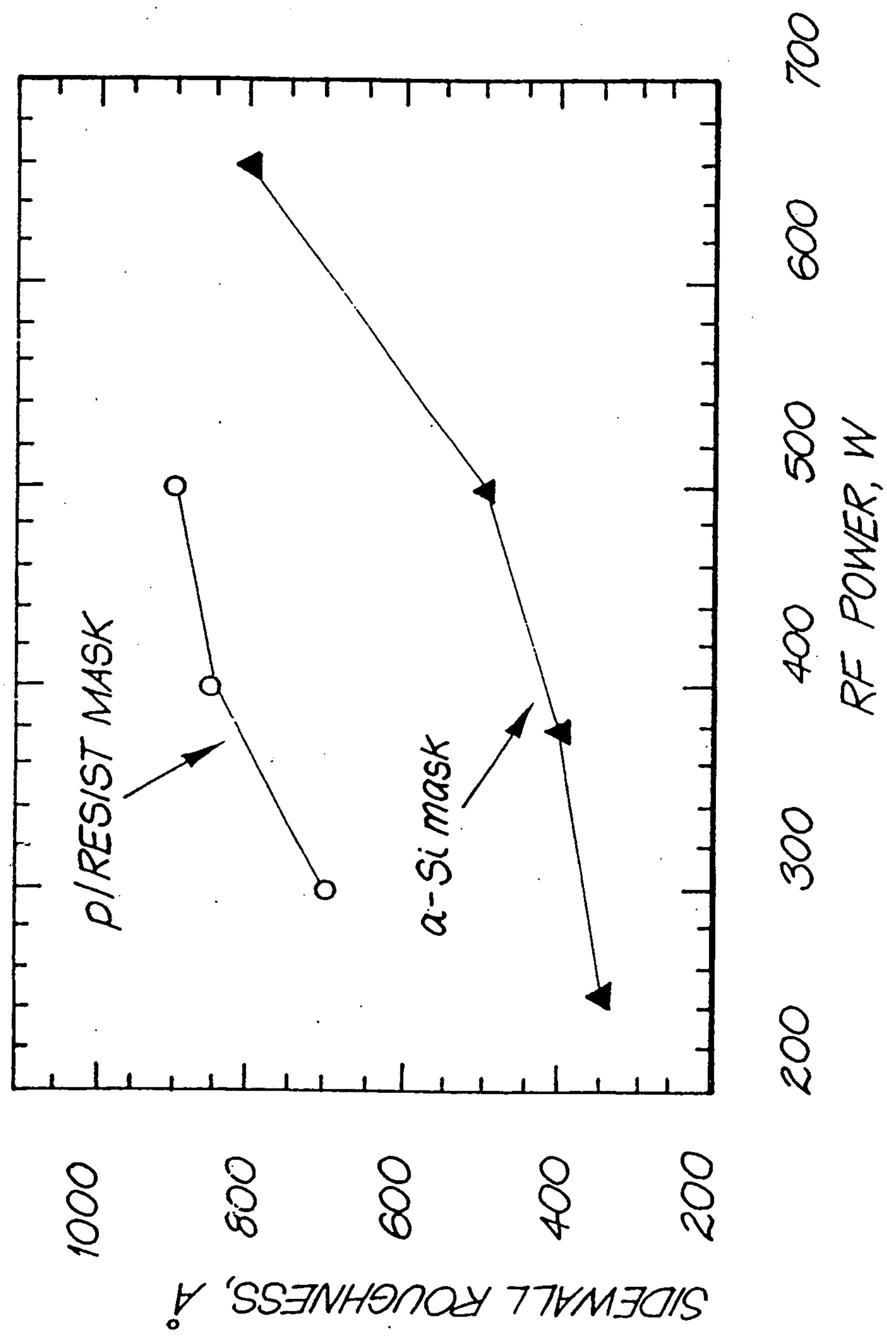

SIDEWALL ROUGHNESS, Å
1000
800
600
400
200
RF POWER, W
200
300
400
500
600
700
p/RESIST MASK
a-Si mask

FIG. 3C

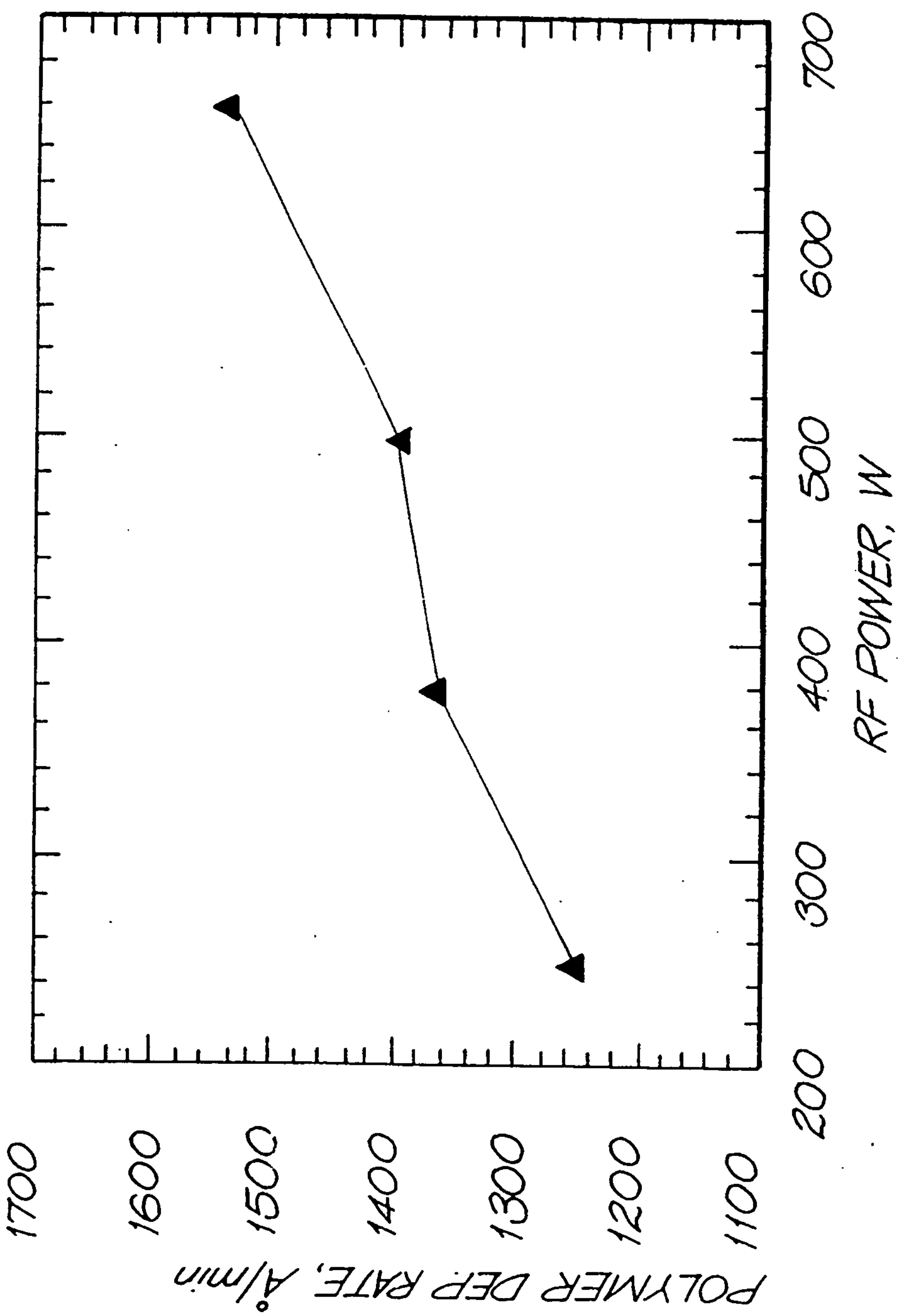

1700
1600
1500
1400
1300
1200
1100
POLYMER DEP RATE, Å/min
200
300
400
500
600
700
RF POWER, W

FIG. 3d

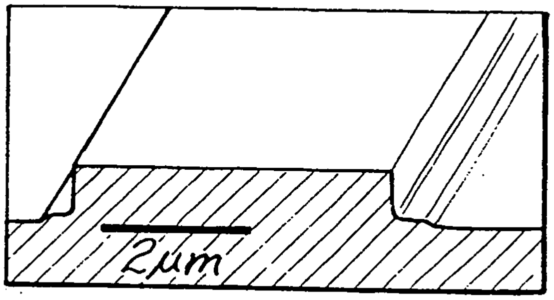


FIG. 4a

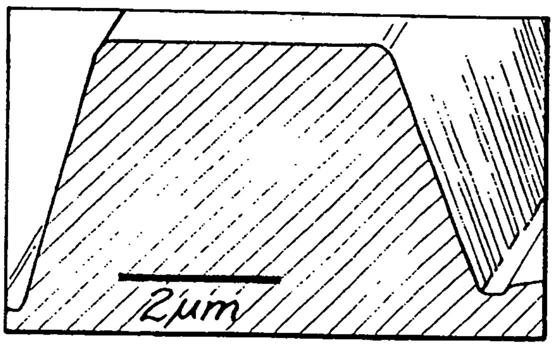


FIG. 4b

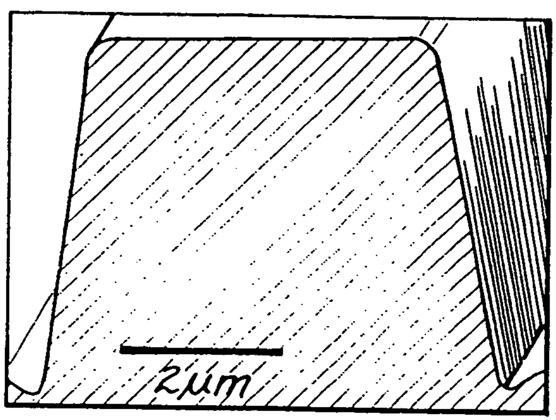


FIG. 4c

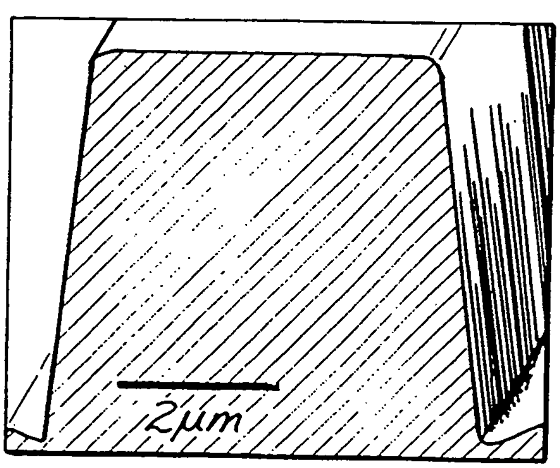


FIG. 4d

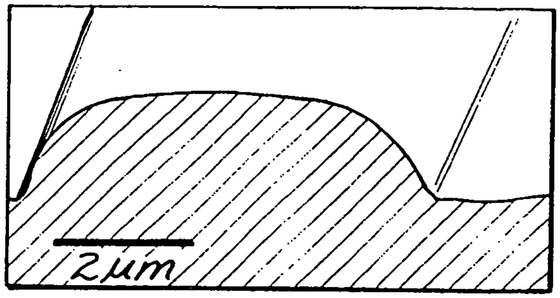


FIG. 4e

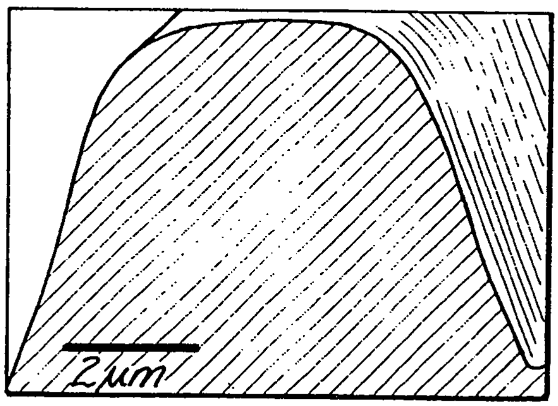


FIG. 4f

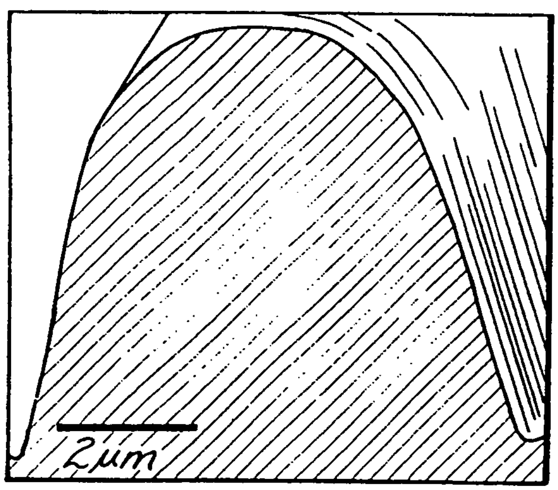


FIG. 4g

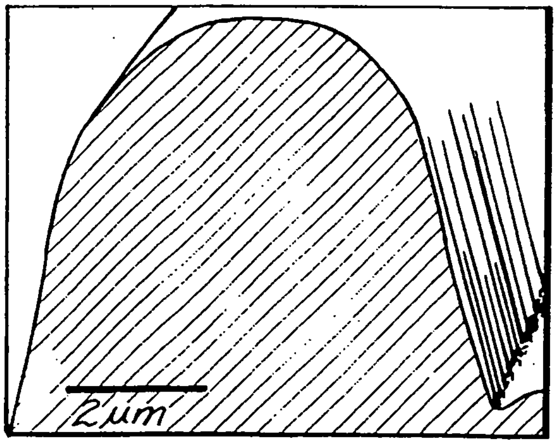


FIG. 4h

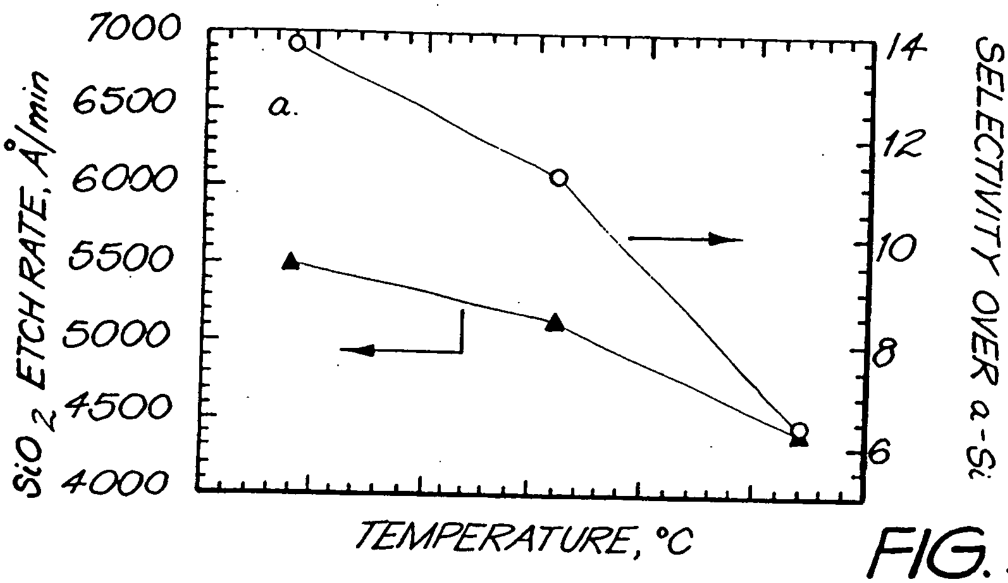


FIG. 5a

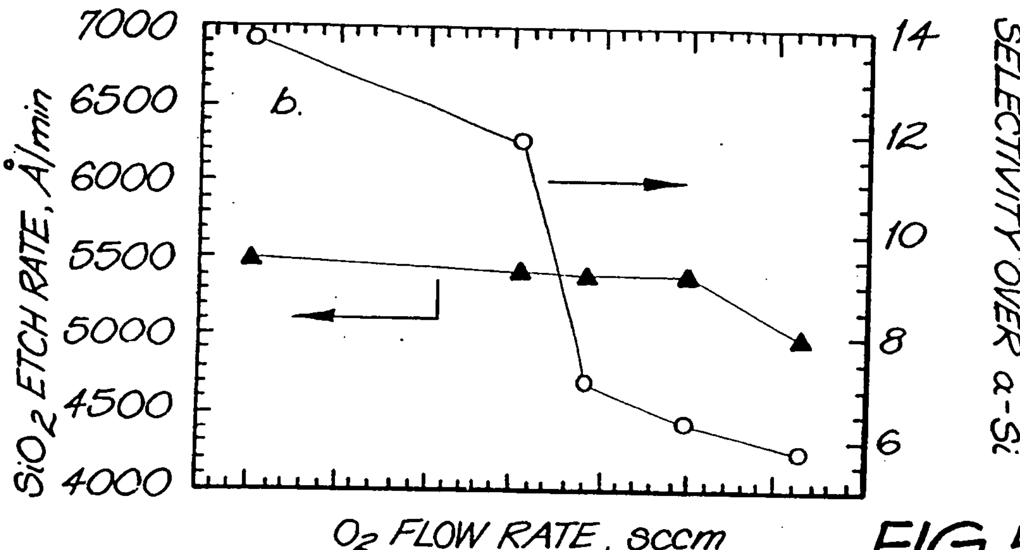


FIG. 5b

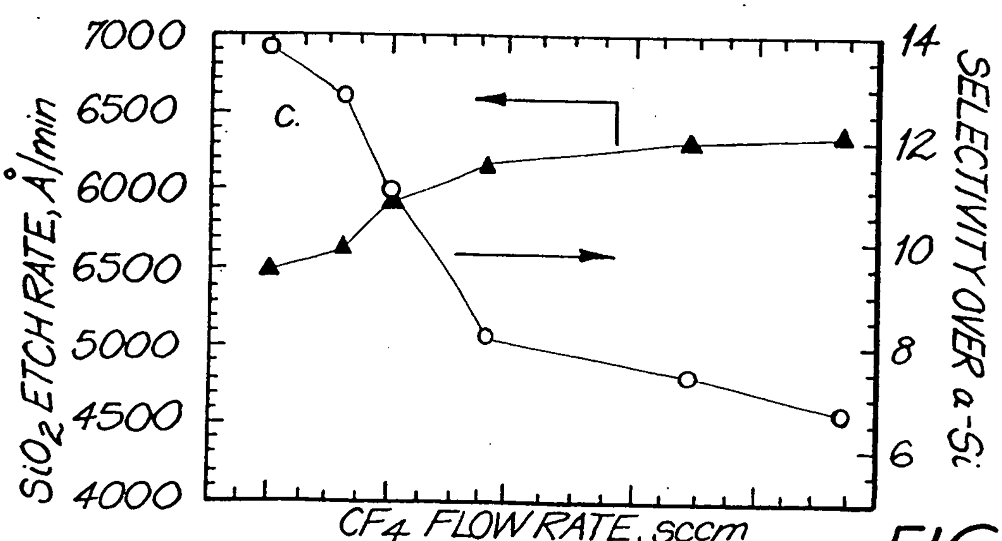


FIG. 5c

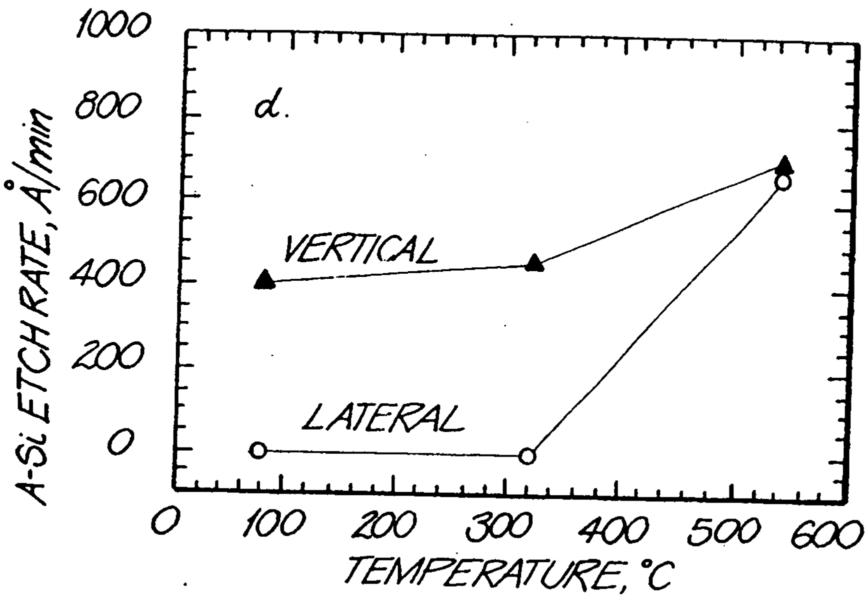


FIG. 5d

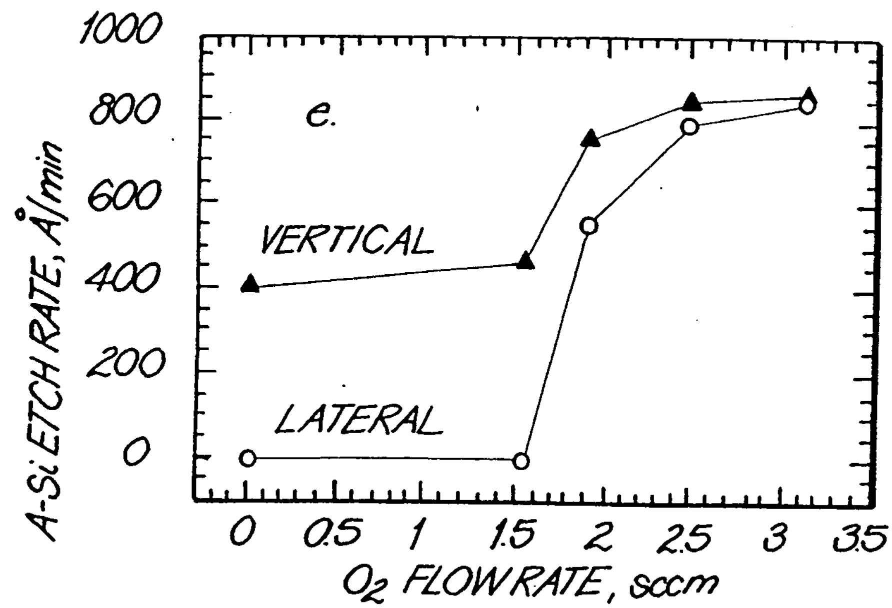


FIG. 5e

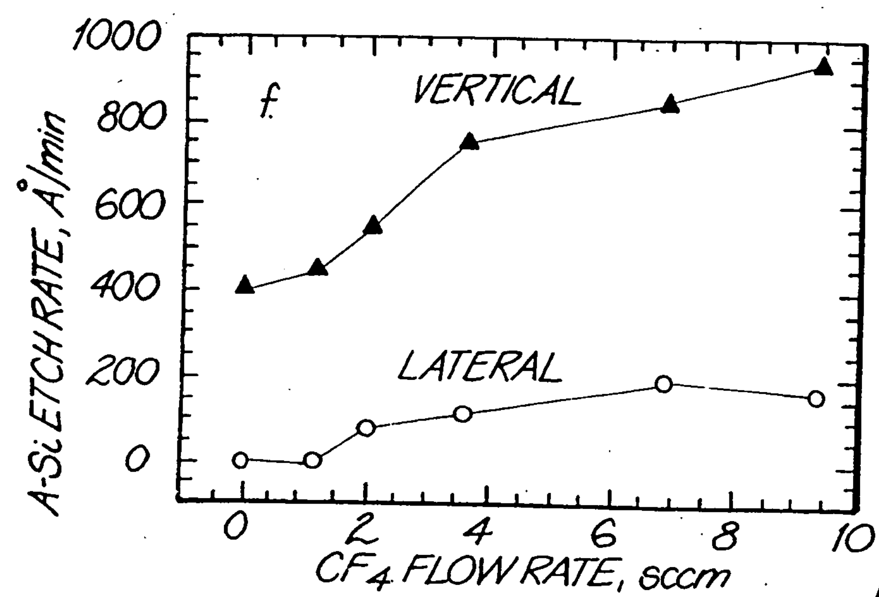
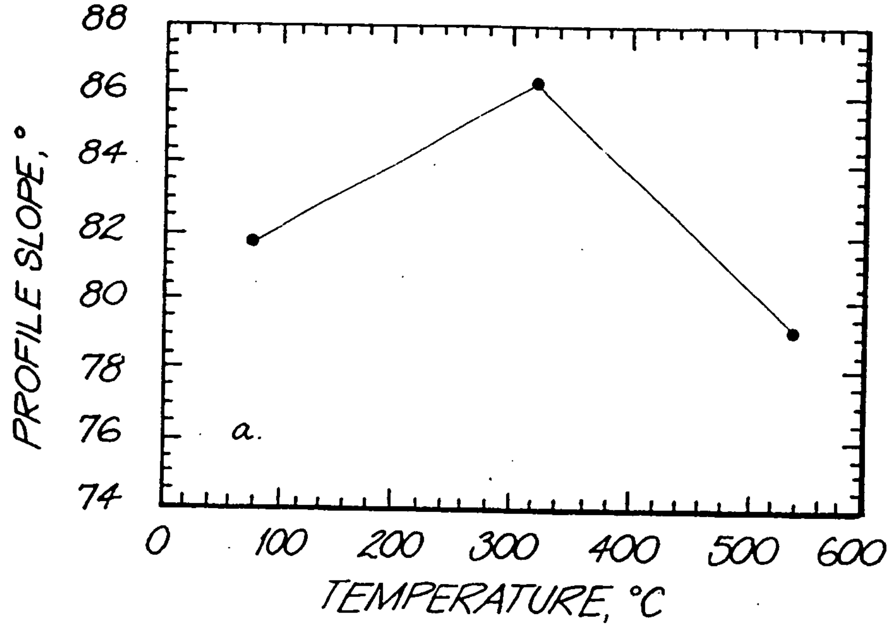
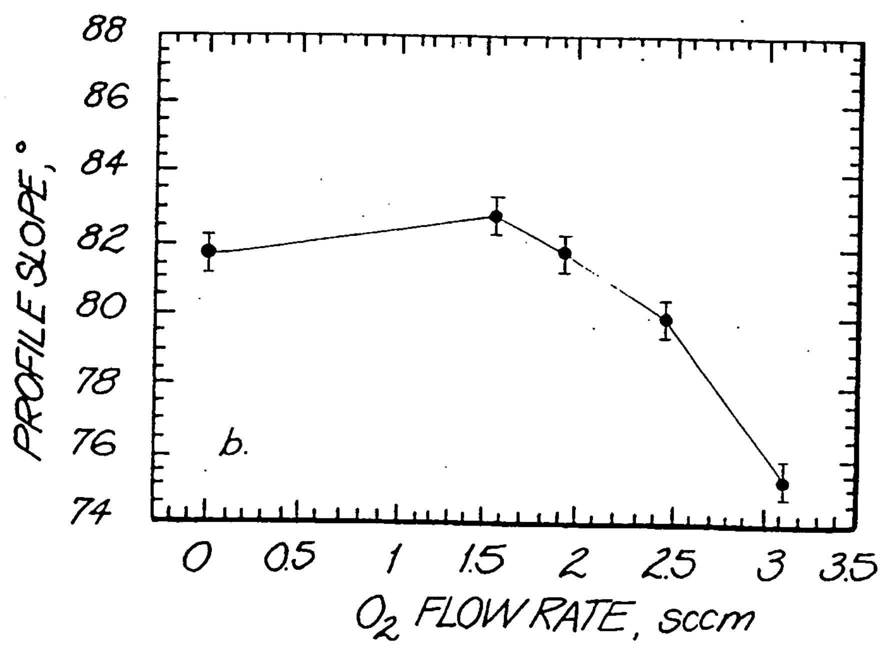


FIG. 5f



88
86
84
82
80
78
76
74
PROFILE SLOPE, °
a.
0
100
200
300
400
500
600
TEMPERATURE, °C

FIG. 6a



88
86
84
82
80
78
76
74
PROFILE SLOPE, °
b.
0
0.5
1
1.5
2
2.5
3
3.5
O_2 FLOW RATE, sccm

FIG. 6b

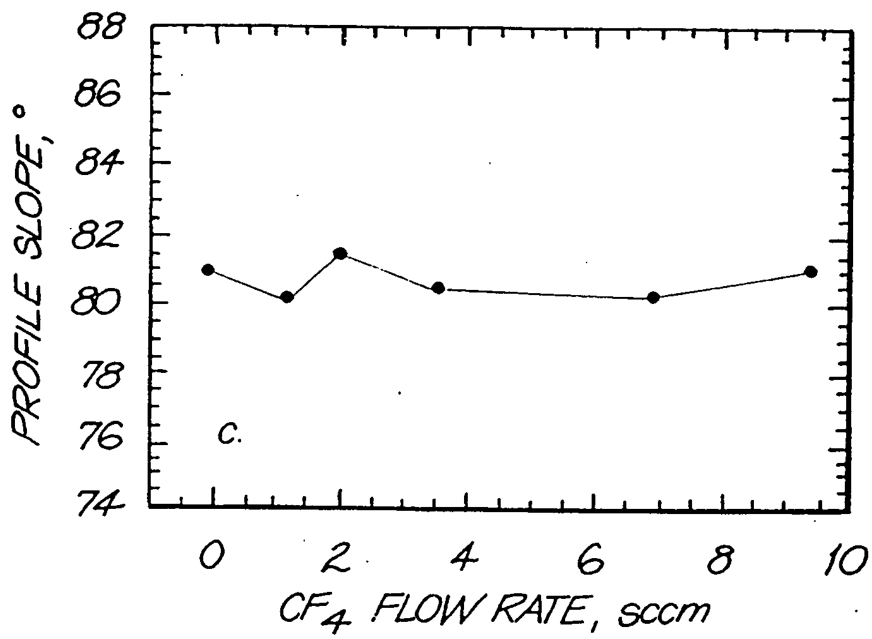

PROFILE SLOPE, °
88
86
84
82
80
78
76
74
c.
0
2
4
6
8
10
CF_4 FLOW RATE, sccm

FIG. 6c

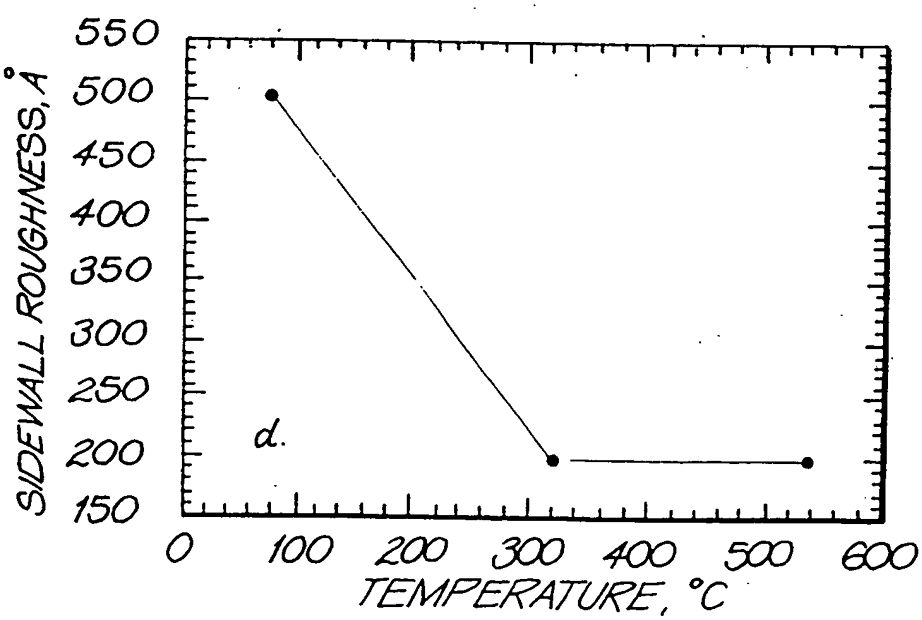

SIDEWALL ROUGHNESS, Å
550
500
450
400
350
300
250
200
150
d.
0
100
200
300
400
500
600
TEMPERATURE, °C

FIG. 6d

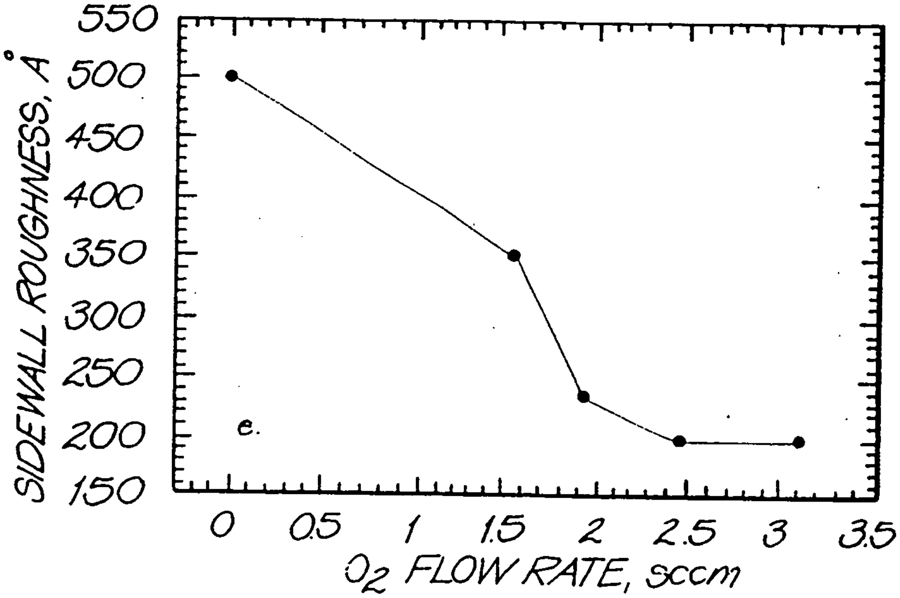

SIDEWALL ROUGHNESS, Å
550
500
450
400
350
300
250
200
150
e.
0
0.5
1
1.5
2
2.5
3
3.5
O_2 FLOW RATE, sccm

FIG. 6e

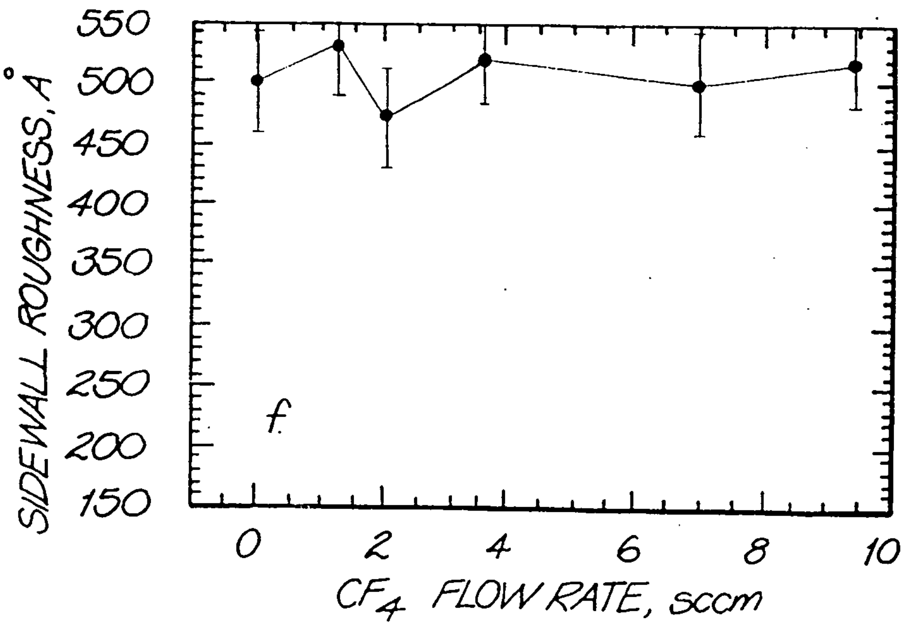

SIDEWALL ROUGHNESS, Å
550
500
450
400
350
300
250
200
150
f.
0
2
4
6
8
10
CF_4 FLOW RATE, sccm

FIG. 6f

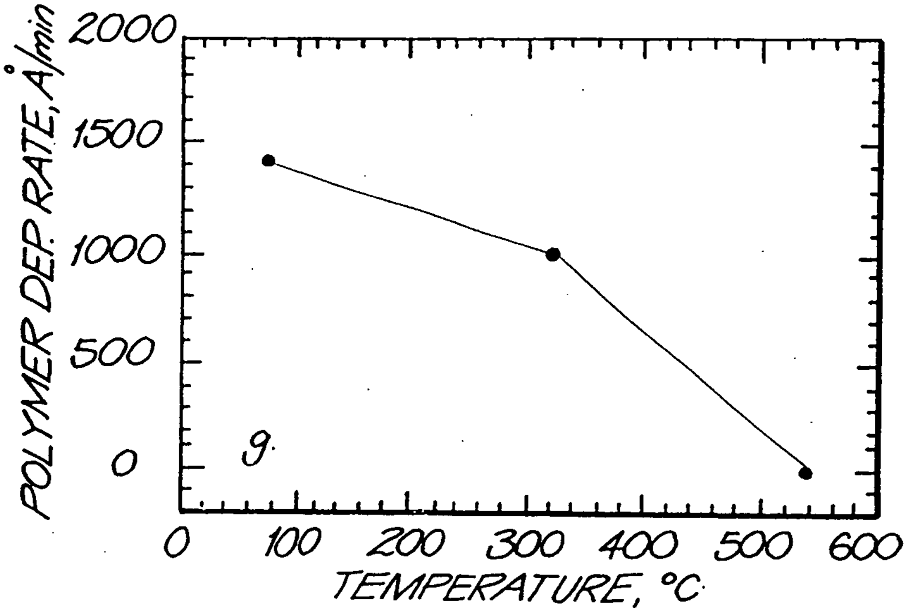


FIG. 6g

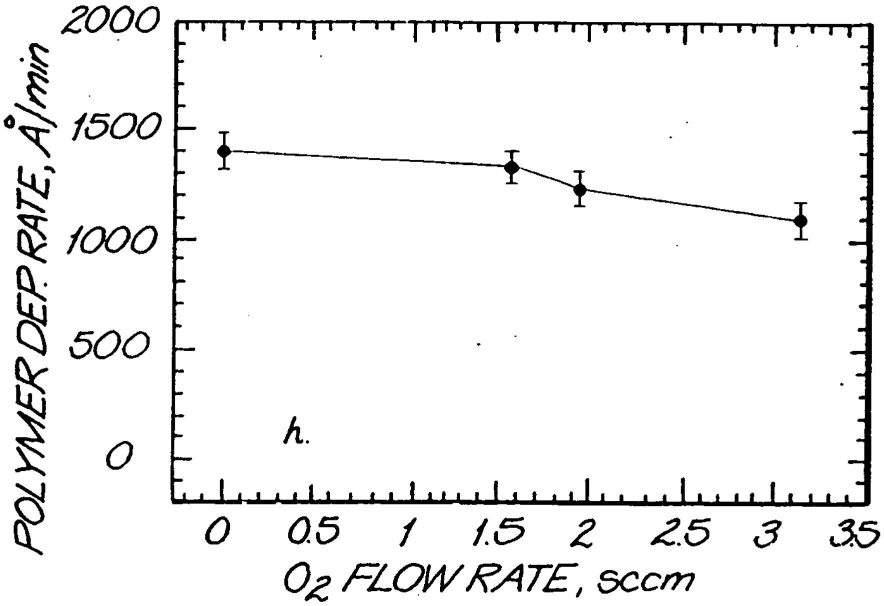


FIG. 6h

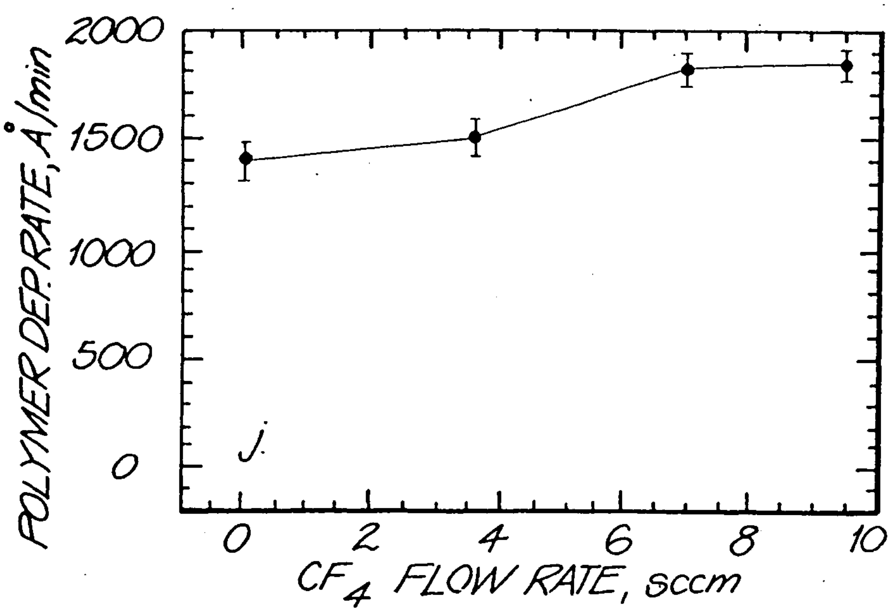


FIG. 6j

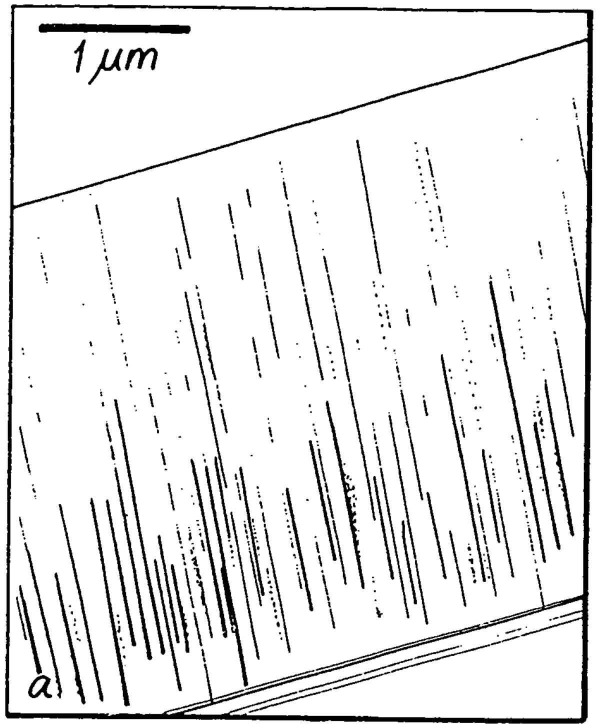


FIG. 7a

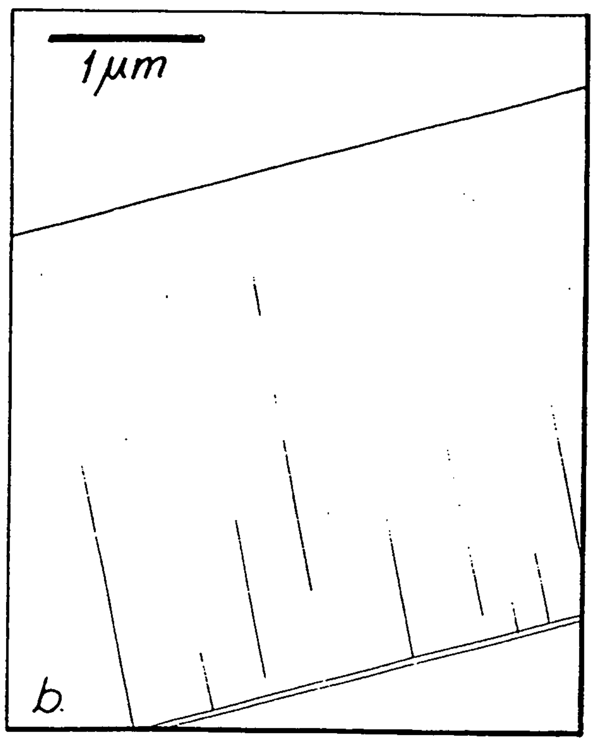


FIG. 7b

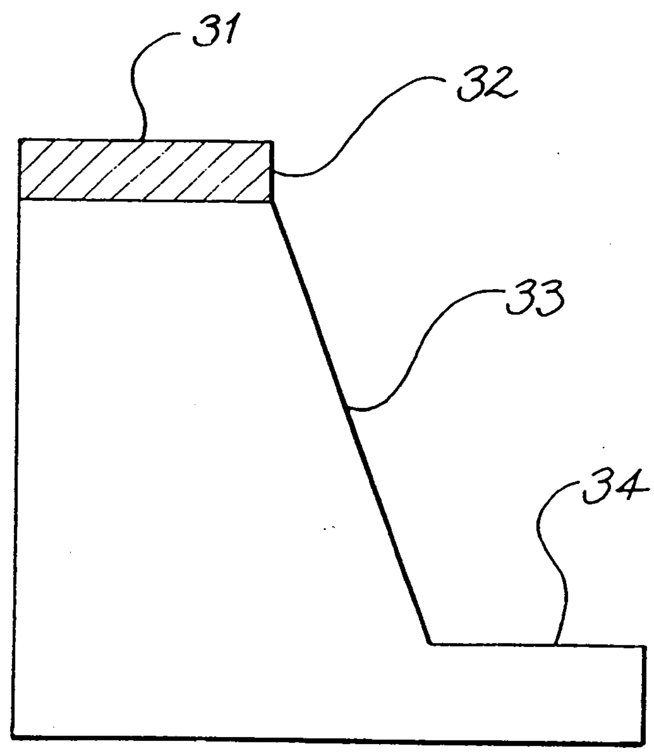


FIG. 8

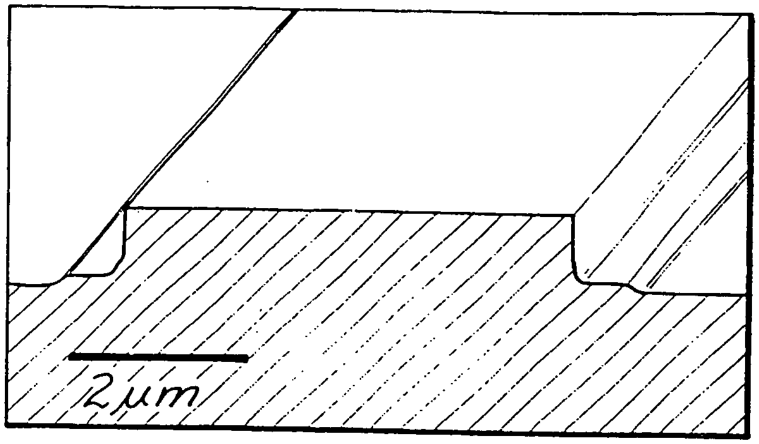


FIG. 9a

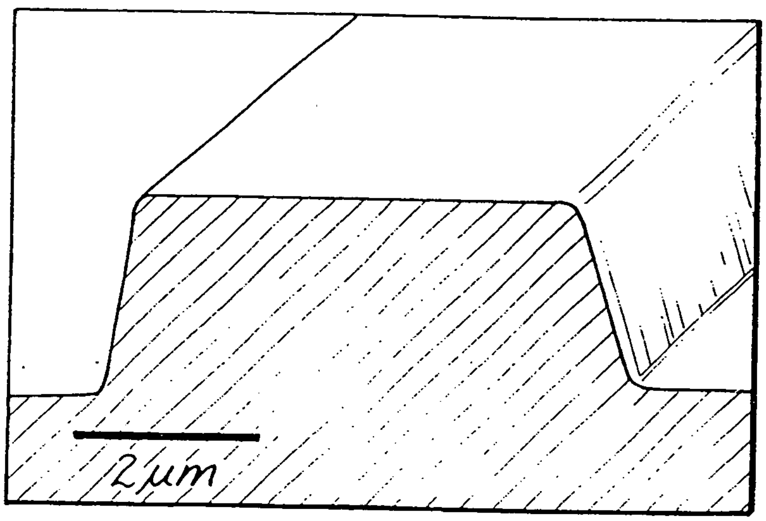


FIG. 9b

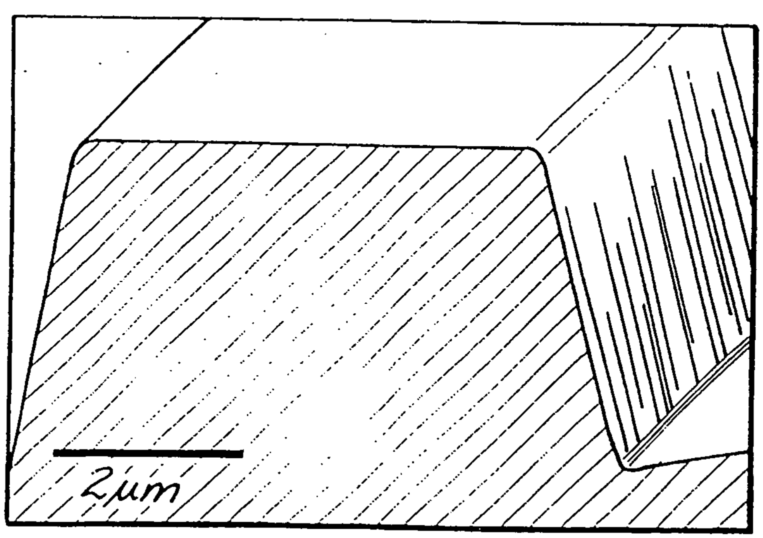


FIG. 9c

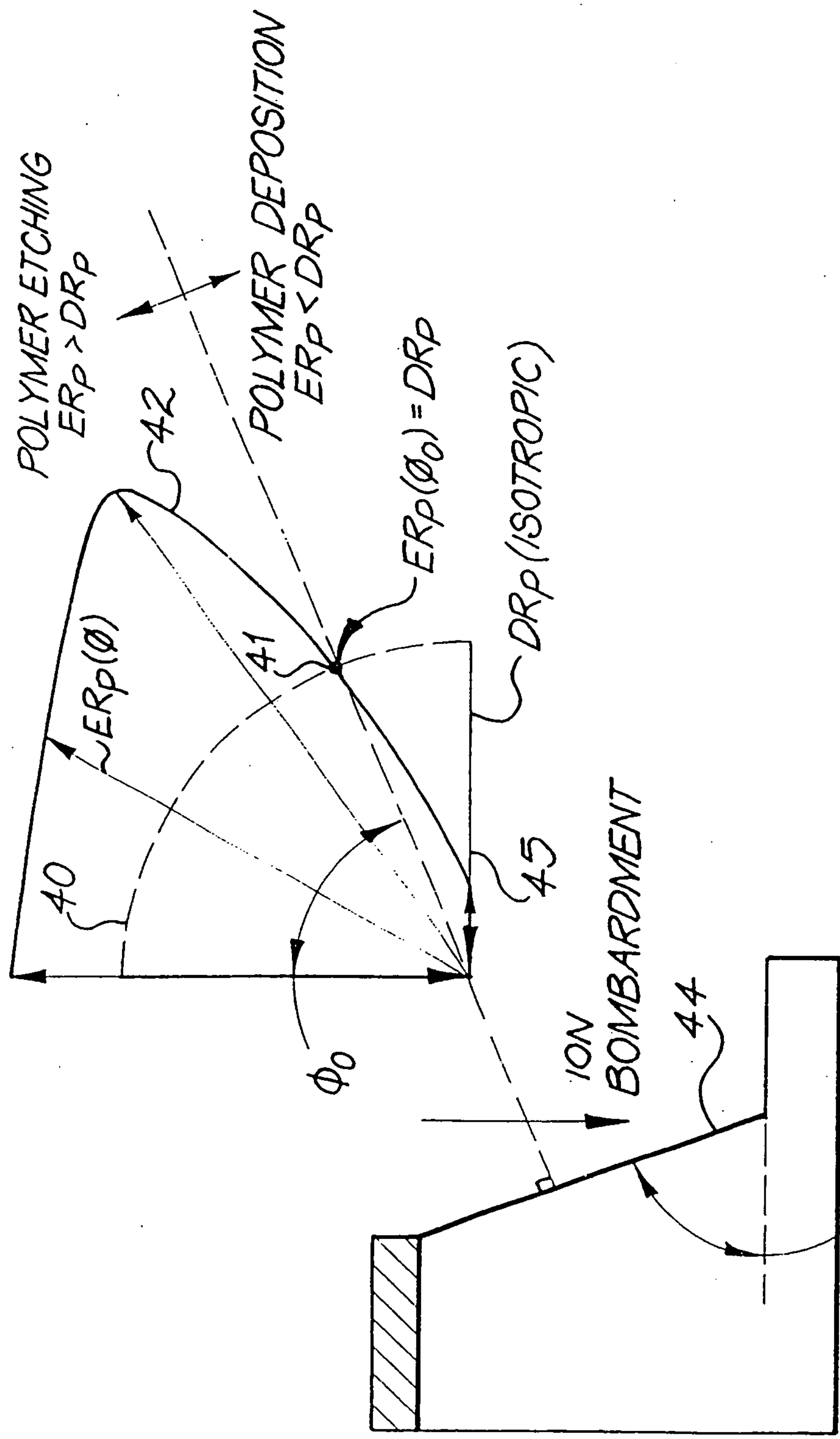

POLYMER ETCHING
$ER_P > DR_P$
POLYMER DEPOSITION
$ER_P < DR_P$
42
$ER_P(\phi_0) = DR_P$
DR_P (ISOTROPIC)
41
$ER_P(\phi)$
40
45
ϕ_0
ION BOMBARDMENT
44
ϕ_0

FIG. 10

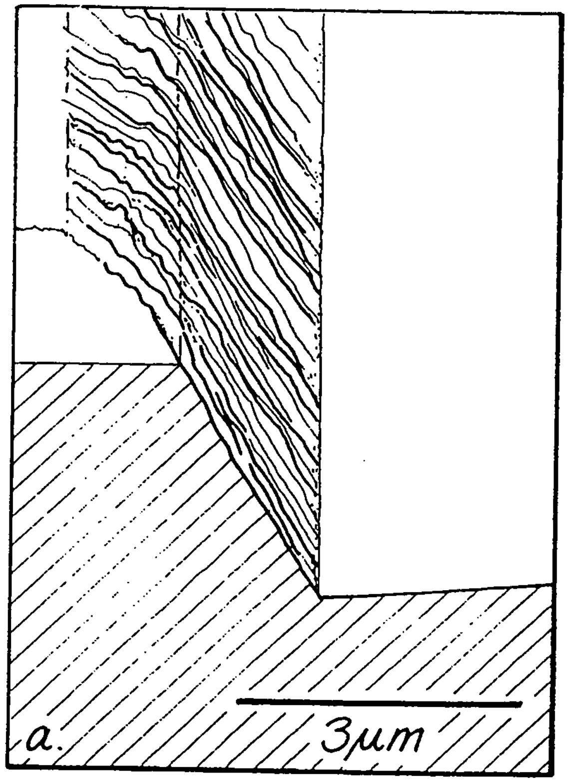


FIG. 11a

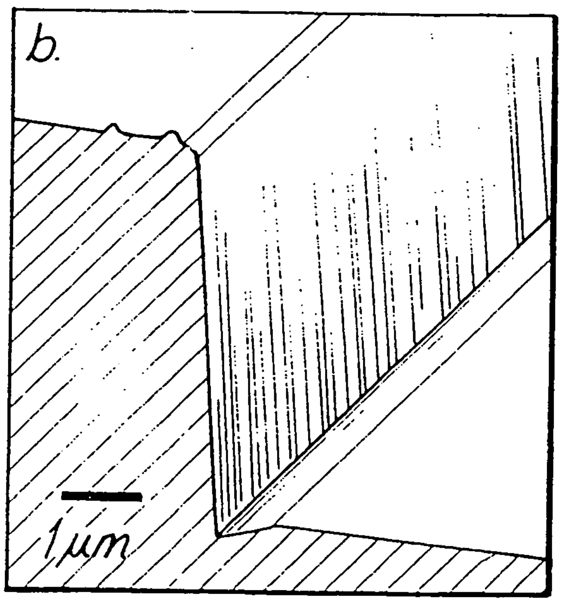


FIG. 11b

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 97/00663

A.	CLASSIFICATION OF SUBJECT MATTER
Int Cl[6]:	C03C 15/00, 17/32; C23C 14/04, 14/12, 14/32, 14/54; G02B 6/136, 6/13, 6/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: C03C 15/00, 17/32; C23C 14/04, 14/12, 14/32, 14/54; C23C 13/04, 13/06, 13/08; G02B 6/136, 6/13, 6/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
AU:IPC as bove

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DERWENT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 482 427 a (HIROYUKI KIRAOKA) 13 November 1984 whole document	1, 4-10, 13
X	US 4 452 665 A (HIROYUKI HIRAOKA) 5 June 1984 whole document	1-10, 13
X	US 5 445 710 A (MASARU HORI et al) 29 August 1995 whole document	1-10, 13

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 November 1997	01 DEC 1997

Name and mailing address of the ISA/AU	Authorized officer
AUSTRALIAN INDUSTRIAL PROPERTY ORGANISATION PO BOX 200 WODEN ACT 2606 AUSTRALIA Facsimile No.: (02) 6285 3929	R.A.K.D. [signature] R. A. K. DIAS-ABEYGUNAWARDENA Telephone No.: (02) 6283 2141

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/AU 97/00663

C (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	"HOLLOW CATHODE ETCHING AND DEPOSITION", JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY, C. M. HORWITZ et al, Vol 6 1988 pages 1937-1844	1-13
A	US 4 460 435 A (Jer-shen Maa) 17 July 1984	
A	EP 010657 A (GENERAL ELECTRIC COMPANY) 14 May 1980	

INTERNATIONAL SEARCH REPORT
Information on patent family members

International Application No.
PCT/AU 97/00663

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	5445710	US	5240554	US	5302240		
US	4482427	DE	3583308	EP	163074	JP	60251628
US	4452665	DW	3486011	EP	154675	JP	60083332
US	4460435						
EP	010657	DE	2967224	EP	10657	US	4209356

END OF ANNEX